The Competitive Semiconductor Manufacturing Survey: Third Report on Results of the Main Phase

Robert C. Leachman, Editor

Report CSM-31

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Executive Summary
by Robert C. Leachman

This document reports the results of the first three and one half years of the Main Phase of the Competitive Semiconductor Manufacturing (CSM) survey. The survey is one component of a multi-year research program to study competitive semiconductor manufacturing worldwide. The study is a joint project of the College of Engineering, the Haas School of Business, the Institute of Industrial Relations and the Berkeley Roundtable on the International Economy at the University of California at Berkeley, under sponsorship of the Alfred P. Sloan Foundation and with the cooperation of semiconductor producers from Asia, Europe and the United States. Professors David A. Hodges and Robert C. Leachman are the project's Co-Directors. Additional funding for this program has been received from Sematech, the Electronics Industry Association of Japan (EIAJ), and the Semiconductor Industry Research Institute of Japan (SIRIJ).

U.C. Berkeley researchers performing this study are faculty, graduate students and research staff from the Schools of Engineering and Business, and from the Department of Economics. Many of the participating firms are represented on the project's Industry Advisory Board, which has played an important role in refining the research agenda.

The first three and one half years of the Main Phase survey of the CSM program involved the measurement of manufacturing performance and investigation of underlying determinants of performance at twenty eight wafer fabrication facilities in the United States, the United Kingdom, Germany, Spain, Japan, Korea and Taiwan. The companies operating these facilities are displayed in Table S-1.

Our basic procedure in the Main Phase survey is to first send participants a one hundred page Mail-Out Questionnaire (MOQ), in which participants document their clean room size and class, head_counts, equipment counts, wafer starts, die yields, line yields, cycle times, computer systems, etc. over the last four years. From the completed MOQs, we calculate technical metrics of manufacturing performance for each of the participants. We then rank the participants for each of the metrics.

We observed a great disparity in the scores of the various participants. In an attempt to understand what practices account for such performance differences, we scheduled a two-day site

Table S-1
List of Companies Participating in the Main Phase of the Competitive Semiconductor Manufacturing Survey (first 3.5 years)

Advanced Micro Devices, Inc. (AMD)
Cypress Semiconductor, Inc.
Delco Electronics Corp.
Digital Equipment Corp. (DEC, 2 fabs)
Harris Corporation
Hyundai Electronics Industries, Ltd.
Intel Corporation
International Business Machines, Inc. (IBM)
ITT Intermetall
LSI Logic Corp. (2 fabs)
Lucent Technologies (2 fabs)
Motorola, Inc.
National Semiconductor Corp. (2 fabs)
Nippon Electronics Corp. (NEC)
Oki Electric Industry, Ltd.
Samsung Electronics Co., Ltd.
Silicon Systems, Inc. (SSI)
Sony Microelectronics Corp. (2 fabs)
Taiwan Semiconductor Manufacturing Corp. (TSMC)
Texas Instruments, Inc.
Tohoku Semiconductor Corp. (TSC)
Toshiba Corp.
United Microelectronics Corp. (UMC)

visit with each participant, during which we toured the manufacturing line, interviewed a cross-section of the entire fab staff, and held a series of sessions to ascertain the fab's strategies for improving yields, improving wafer throughput, reducing cycle times, etc., and to survey its development of resources for improvement such as computer integrated manufacturing (CIM) and information systems, human resources development, deployment of work groups and teams, etc. These more qualitative data concerning the participants' operational practices were then correlated with the metric scores in order to identify those practices that underlie top performance.

In this report, the values of ten technical metrics of semiconductor manufacturing performance are presented for the participants. We also compare and contrast managerial, organizational and technical practices underlying performance at the participants. Performance and practice comparisons are separated into three categories according to the type and sophistication of devices that are fabricated. We define fab categories for submicron memory products, CMOS logic products with feature sizes smaller than 1.5 microns, and medium scale integration (MSI) products such as analog circuits and power devices. The particular identities of the participating fabs are not revealed. Instead, the fabs are consistently identified throughout the report using labels M1, M2, M3, etc. for memory fabs, L1, L2, L3, etc. for CMOS logic fabs, and B1, B2, B3, etc. for MSI fabs.

Metrics of Manufacturing Performance

The technical metrics used to measure manufacturing performance of the participants are summarized as follows:

(1) Average line yield per twenty mask layers.

(2) Defect densities, calculated for major process flows in each fab by plugging reported die yields and die sizes into the Murphy model of defect density. The reported defect densities account for all yield losses, including both spot defects and parametric problems. For memory products, the die yields applied to the defect density formula are final die yields after laser repair.

(3) Integrated fab and die sort yield, calculated as the product of line yield per twenty masking layers and the estimated die yield for a 0.5 sq cm die. This die yield is estimated using the Murphy defect density calculated from reported die yields as described above.

(4) Wafer masking layers completed per 5X stepper per calendar day (considering only layers exposed using 5X steppers).

(5) Wafer implant layers completed per ion implanter per calendar day.

(6) Wafer metal layers completed per metallization machine per calendar day.

(7) Integrated 5X stepper throughput, the equivalent number of full-wafer operations per 5X stepper per day, calculated as the number of 5X wafer operations per day times the integrated yield defined in (3) above.

(8) Average cycle time per mask layer.

(9) Wafer masking layers completed per operator per working day (considering all masking layers, regardless of type of lithography equipment).

(10) Wafer masking layers completed per working day divided by the total head count.

For all of these metrics, we encountered a wide range in scores, even though the basic process technology in use at the participants was generally similar. Tables S-2, S-3 and S-4 summarize the best, average, and worst scores for each metric for the three fab categories, considering the latest data points we received from each of the twenty eight participants. These data points represent measurements of manufacturing performance in some quarter between the middle of 1992 and the middle of 1995, depending upon the participant.

Rates of improvement were studied for each participant, whereby scores for each technical metric were computed for each quarter over a period of three to four years. For most metrics, the ranking of participants is generally constant, i.e., we did not find many cases where a last-place participant overtook the leader for a particular metric, although a few participants improved their rankings considerably over the period.

One of the most striking trends we observed in our measurements concerns the initial defect densities for process flows, i.e., the defect densities realized in the first quarter after transfer of the process flow into manufacturing. We recorded a factor-of-ten range in initial defect densities. Those fabs with poor starting points tend to have faster rates of improvement, but not nearly fast enough to overtake those with good starting points, at least not for several years, as those with good starting points also make steady if somewhat slower progress reducing defect densities.

The integrated stepper throughput metric is perhaps our best indicator of overall fab productivity, at least for submicron fabs dependent on this technology for photolithography. The varying strengths and weaknesses in line yield, die yield (defect density) and stepper throughput among our participants are integrated to see the overall throughput of good silicon per machine. Even for such an integrated metric, we find a remarkable factor-of-seven range in performance.

Practices Underlying Manufacturing Performance

Our main objective in the CSM survey is to identify those operational practices that underlie leading-edge manufacturing performance. Summarized below are the operational practices that distinguish those fabs achieving best or near-best scores in one or several of the metrics described above. (For the sake of brevity, we refer to such fabs as the "leading" fabs.) But before summarizing our findings in that regard, it is only fair to acknowledge that our analysis does not account for several strategic factors concerning product design and fab design that may strongly influence manufacturing performance.

First, the restrictiveness of product design rules can have a strong influence on observed die yields and hence on our calculated defect densities. We made no attempt to normalize defect density scores for potential differences in design rules among the participants.

Second, the range of sizes of fabs in our survey, in terms of wafer starts, spans a factor of almost fifty. Small fabs generally have inferior labor and equipment productivity scores, because of the indivisibility of machines and personnel, and because of the tendency to install extra equipment to avoid situations in which a particular process step must be performed by a one-of-a-kind equipment type. In the tables and graphs of metric scores in this report, we made no attempt to normalize productivity scores to account for fab size, but we provide a general assessment here. Let us define a general categorization of our participants into large, medium and small fabs,

Table S-2
Summary of Technical Metric Scores for Memory Fabs,
Competitive Semiconductor Manufacturing Survey (1992-1995)

Metric	Best Score	Average Score	Worst Score
Line yield per twenty layers (%)	98.8	93.0	87.1
Murphy defect density - 0.45 - 0.6 micron CMOS memory (defects per sq cm after repair)	0.03	0.59	1.34
Murphy defect density - 0.7 - 0.9 micron CMOS memory (defects per sq cm after repair)	0.01	0.51	1.81
Murphy defect density - 1.0 - 1.25 micron CMOS memory (defects per sq cm after repair)	0.31	0.59	1.08
Integrated fab and sort yield (%) 0.45 - 0.6 micron CMOS memory (0.5 sq cm device)	91.7	72.1	46.0
Integrated fab and sort yield (%) 0.7 - 0.9 micron CMOS memory (0.5 sq cm device)	92.9	73.9	35.9
Integrated fab and sort yield (%) 1.0 - 1.25 micron CMOS memory (0.5 sq cm device)	77.0	66.7	48.3
5X Stepper throughput (wafer operations per 5X stepper per day)	606	463	281
Ion implanter throughput (wafer operations per implanter per day)	1,360	855	339
Metallization throughput (wafer operations per machine per day)	273	147	53
Integrated 5X stepper throughput (Equiv. full-wafer operations per stepper per day)	479	344	160
Cycle time per mask layer (days)	1.8	2.9	4.1
Direct labor productivity (mask layers completed per operator per day)	71.7	42.6	18.4
Total labor productivity (mask layers completed per total headcount per day)	51.6	27.3	15.1

Table S-3
Summary of Technical Metric Scores, CMOS Logic Fabs
Competitive Semiconductor Manufacturing Survey (1992-1995)

Metric	Best Score	Average Score	Worst Score
Line yield per twenty layers (%)	97.2	89.8	77.8
Murphy defect density - 0.7 - 0.9 micron CMOS logic (defects per sq cm)	0.28	0.74	1.96
Murphy defect density - 1.0 - 1.25 micron CMOS logic (defects per sq cm)	0.23	0.58	2.16
Murphy defect density - 1.3 - 1.5 micron CMOS logic (defects per sq cm)	0.14	0.43	1.07
Integrated fab and sort yield (%) 0.7 - 0.9 micron CMOS logic (0.5 sq cm device)	76.4	63.9	37.8
Integrated fab and sort yield (%) 1.0 - 1.25 micron CMOS logic (0.5 sq cm device)	84.6	71.1	37.5
Integrated fab and sort yield (%) 1.3 - 1.5 micron CMOS logic (0.5 sq cm device)	85.9	71.8	52.1
5X Stepper throughput (5X layers completed per 5X stepper per day)	606	362	140
Ion implanter throughput (wafer operations per implanter per day)	1,146	633	163
Metallization throughput (wafer operations per machine per day)	345	154	34
Integrated 5X stepper throughput (Equiv. full-wafer operations per stepper per day)	469	220	59
Cycle time per layer (days)	1.8	2.7	3.3
Direct labor productivity (wafer layers completed per operator per day)	43.4	23.7	5.5
Total labor productivity (wafer layers completed per total headcount per day)	27.6	14.6	2.7

Note: Average and worst scores are calculated for certain metrics after discarding the worst data point in our sample.

Table S-4
Summary of Technical Metric Scores, Medium Scale Integration Fabs
Competitive Semiconductor Manufacturing Survey (1992-1995)

Metric	Best Score	Average Score	Worst Score
Line yield per twenty layers (%)	91.2	77.7	65.9
Murphy defect density - 1.5 - 4.0 micron CMOS and BiCMOS logic (defects per sq cm)	0.89	1.45	2.24
Murphy defect density - 1.2 - 3.5 micron Bipolar (defects per sq cm)	0.09	1.30	3.09
Murphy defect density - 5.0 - 10.0 micron Bipolar (defects per sq cm)	0.79	1.82	2.98
Integrated fab and sort yield (%) 1.5 - 4.0 micron CMOS and BiCMOS (0.5 sq cm device)	51.7	38.5	28.4
Integrated fab and sort yield (%) 1.2 - 3.5 micron Bipolar (0.5 sq cm device)	88.1	51.0	20.6
Integrated fab and sort yield (%) 5.0 - 10.0 micron Bipolar (0.5 sq cm device)	45.1	32.9	21.5
5X Stepper throughput (5X layers completed per 5X stepper per day)	724	478	231
Ion implanter throughput (wafer operations per implanter per day)	627	227	128
Metallization throughput (wafer operations per machine per day)	172	72	31
Cycle time per layer (days)	1.2	2.6	3.7
Direct labor productivity (wafer layers completed per operator per day)	46.6	24.5	9.9
Total labor productivity (wafer layers completed per total headcount per day)	27.1	14.6	6.3

Note: Average and worst scores are calculated for certain metrics after discarding the worst data point in our sample.

where large fabs make more than 7,000 wafer starts per week, medium fabs make 2,500 - 7,000 wafer starts per week, and small fabs make less than 2,500 wafer starts per week. Large fabs dominate almost every one of our labor and equipment productivity metrics, although fab size above 7,000 wafer starts per week does not distinguish performance. In the yield and defect density metrics, small and medium size fabs are competitive with the large fabs.

Third, the assignment of older-generation processing equipment to newer-generation process flows may make the achievement of world-class defect densities much more difficult than the achievement possible with the assignment of newer equipment. While yields may be lower for the strategy to employ older processing equipment, capital costs are lower as well, and so the strategy might turn out to be economically competitive or even superior to the strategy that employs solely new processing equipment. We made no attempt to normalize defect density scores for the generations of equipment applied.

With these strategic factors aside, we now summarize the various operational practices we found to be correlated with good manufacturing performance (in terms of the manufacturing metrics we have defined). We define eight basic themes for key practices that underlie leading performance. In short, these themes are as follows:

1. Make manufacturing mistake-proof.

2. Integrate process, equipment and product data, and analyze it statistically.

3. Automate information handling and step-level material handling.

4. Develop a problem-solving organization.

5. Reduce the division of labor.

6. Secure the requisite technical talent.

7. Manage new process introductions.

8. Schedule manufacturing activity.

The first theme *(Make manufacturing mistake-proof)* concerns practices that ensure the manufacturing process is executed correctly. Some participants with a narrow product mix and very disciplined, well-trained operators are able to achieve high line yields with little or no automation. But other leading participants have applied very effective forms of automation -- emphasizing automation of *information* handling rather than automation of *material* handling -- that serve to make manufacturing very mistake-proof. Such automation includes procedural checks that require the right production lot and the right machine to be selected before processing activity may be initiated, and automated download of the machine recipe (i.e., the processing parameters) to the processing machines. Fabs using this kind of automation achieve outstanding line yields, even when producing a broad range of products in a variety of process flows, and

even when coping with high rates of operator turnover. We find it remarkable that several otherwise well-run fabs suffered significant line yield losses primarily because of mis-processing events, e.g., a process step was skipped or duplicated, the wrong recipe was input to the machine, processing activity continued even though an out-of-control situation was detected using statistical process control (SPC), etc.

Good process control systems do not make manufacturing strictly mistake-proof, but they serve to contain losses to minimal levels. All fabs in our survey apply SPC to their processes and equipment. The leading fabs make considerable use of sensors and computers to monitor equipment performance, and provide automated notification of out-of-control conditions and on-line assistance for trouble-shooting.

Following the second theme *(Integrate and analyze data),* the leading fabs utilize computerized tracking systems to achieve excellent data collection and excellent data analysis capabilities. They collect large amounts of data concerning process and product conditions (an activity termed engineering data collection, or "EDC"), equipment maintenance and operation history, lot production history, and yield results. They integrate these data in a single relational database. Statistical tools are routinely applied to these data by process engineers, enabling them to expeditiously pinpoint causes of low die yields and make rapid deployment of counter-measures to contain losses. Wafer maps of the results of in-line defect inspections are used extensively in the leading fabs, as are end-of-line wafer maps of die yield and of memory bit fails.

The leading fabs rigorously measure the overall equipment efficiency (OEE) of their key processing equipment, identifying losses in throughput and prioritizing needed improvements. In the best fabs, equipment status is automatically captured from machine logs using SECSII interfaces. Actual processing time is automatically monitored and compared against engineering standards; alarms are triggered when elapsed times are excessive.

The third theme *(Automate information handling and step-level material handling)* concerns automation of much of the overhead surrounding the performance of processing steps. Automation of information handling includes procedural checks and auto-recipe download as described above. It also includes automated capture of engineering data and equipment tracking data using bar codes and sensors, as well as automated notification of operators or technicians when machines are about to become idle or when they require maintenance or attention. Fabs that have automated such information handling are more mistake-proof and thus have superior line yields, they have much higher-quality and more timely engineering and production data and thus superior die yield improvement efforts, and their equipment throughputs and labor productivities are much higher.

Material handling automation efforts may be divided into three types: interbay automation, intrabay automation, and step-level automation. Interbay automation concerns the movement of production lots between equipment bays using automated guided vehicles (AGVs) or overhead railroads to haul lots between stockers serving the bays. Intrabay automation concerns the movement of lots between stockers and processing machines in the bay using AGVs or traveling robot arms. Step-level automation involves the use of robot arms or tracks to handle wafers or cassettes of wafers between lot box and processing chamber, or between consecutive processing chambers. We find that step-level automation has the greatest positive impact on fab performance among our participants. Fabs that have linked up coat, expose and develop steps in photolithography into

a single operation achieve higher yields and lower cycle times with no diminution of equipment throughput. Application of robotics or other handling automation to wet etch, diffusion, plasma etch, and metallization steps also is associated with superior line yields, cycle times, equipment throughputs and labor productivities in our sample.

Perhaps interbay automation may become essential as the industry moves to larger wafer sizes, but for 150mm wafers their benefit seems to be limited to modest improvements in direct labor productivity. On the other hand, step-level automation provides significant benefits by making manufacturing more controllable and repeatable, and eliminating a much greater portion of the operator's duties. Our sample does not permit us to make an evaluation of intrabay automation, but we conjecture most of its benefits will be associated with automated scheduling and other information automation that must accompany it, rather than with the material handling itself.

The fourth theme *(Develop a problem-solving organization)* means that a successful fab must have an organization that not only executes the manufacturing processes well, but also is very good at problem recognition and at problem solving. Semiconductor manufacturing is characterized by immature processes and immature processing equipment with relatively short lives, and by continuing increases in complexity. Opportunities to improve yields and/or wafer throughput are always present. Thus manufacturing has as much an engineering character as it does an operational character. This means a fab must continually develop technical competence of its organization and continually foster a teamwork approach to recognize problems, devise innovative solutions, and implement them quickly and successfully. Not only engineers but also operators and technicians must participate in problem recognition, process improvement and problem solving, and they therefore must possess basic engineering skills as well as technical knowledge of the manufacturing processes and equipment. The leading fabs have instilled problem-solving skills in their technicians and operators through extensive training, mentorship and participation in continuous-improvement teams organized under the TQM and TPM paradigms. [1]

Following the fifth theme *(Technical talent),* leading fabs have the internal technical talent as well as the requisite support from vendors to expeditiously make modifications to product, process, and equipment in order to implement changes that have been identified by problem solving efforts as desirable or necessary to improve manufacturing performance. In particular, leading fabs have considerable in-house equipment engineering talent, identifying and implementing useful modifications to process equipment that improve performance or ease maintenance. In contrast, weak-performing fabs have process engineering organizations that are virtually devoid of equipment engineering skills.

The sixth theme *(Reduce division of labor)* concerns training efforts and job expansions to reduce response time to problems and to promote more effective formulation of engineering

1. TQM (Total Quality Management) focuses improvement efforts on product quality. TPM (Total Productive Maintenance) focuses improvement efforts on equipment productivity. The two paradigms are thus complementary, and tend to drive different kinds of improvements. While most of the leading fabs had embraced TQM first and then TPM later, this is probably a historical artifact reflecting the relative ages of the paradigms.

solutions. Operators at leading fabs are trained to perform basic equipment maintenance and trouble-shooting, enabling them to be pro-active instead of resigned to wait for a technician when the need for maintenance or correction arises. In such fabs, each equipment bay on every operating shift is staffed with a technician or operator designated as the "key man" or "equipment owner" for that type of processing equipment; this person trains and focuses the rest of the staff for improved equipment operation and maintenance, responds immediately to problems that may arise, and serves as a technical resource and mentor for other operators.

Technicians and operators work together in leading fabs on continuous improvement teams, directed and supported by engineers. Such teams identify and research process and equipment problems, find root causes, and then devise, test and implement permanent fixes. The teams serve to expand the knowledge, skills, confidence and job scope of both technicians and operators.

The division-of-labor theme also applies to engineers. Process and Equipment Engineering groups are merged in leading fabs, broadening the skills of engineers and promoting quicker identification and implementation of effective solutions to process and equipment problems. Rather than being exclusively the domain of Statisticians or of Yield and Integration Engineers, statistical analysis of yield is practiced regularly by Process Engineers at leading fabs.

Under the seventh theme *(Manage new process introductions),* leading fabs have effective procedures for managing the introduction of new process flows. The economic life of many process flows is three to four years, with unit prices for products of the flow declining rapidly over this period. Thus it is economically important to realize high throughput of the process flow early in its life, and to fairly frequently introduce new process flows into the fab. This means the fab must become expert in each new process flow and its required equipment as soon as possible, ideally before it transfers to production, so as to realize good yields and good wafer throughput early in its life and to quickly ramp to better yields and higher wafer throughput thereafter. Even if a fab is proficient in all of the above practices, a poor start with a new flow may leave the fab too far behind to catch up before the market value of the output has mostly drained away.

The leading participants strategically control the number of variables to be managed, staggering transitions to the next product generation and the next process generation, and metering the number of new modules in each process generation to keep the difficulties in each generation to a tractable level.

The leading participants also have effective operational procedures for new process transfer. Equipment sets used in development and in production are duplicated, and development and volume production are often co-located. Transfer of process documentation is electronic. Engineers from the recipient manufacturing fab participate in the final stages of development.

Finally, the eighth theme *(Schedule production activity)* concerns the efforts of fabs to reduce cycle time and improve on-time delivery. The leading fabs utilize automated production planning systems that insure releases of new production lots do not overload fab resources and that target out schedules are consistent with steady flow of work-in-process (WIP) according to target cycle times. Delivery quotations to customers are automatically made on the basis of the planned production. Dispatching of lots on the factory floor is performed to prioritize lots that are behind schedule, supplemented with Kanban controls that ensure WIP is kept in balance.

Practice Trends

Each participant tended to score well or score poorly in most metrics, reflecting the fact that particular practices, good or bad, tend to influence several metrics. Perhaps reflecting the insulation of the participants and their independent efforts to improve manufacturing, almost every participant presented to us at least one good practice that we did not find elsewhere, and whose adoption by the other participants we believe would improve performance.

No single fab is the leader in all eight themes described above. The best integrated database and best statistical yield analysis system we saw was in a Korean fab; the best equipment efficiency analysis system was in a Japanese fab; the best information handling and step-level automation implementation we saw was in a fab in Taiwan; and the best cycle time control and on-time delivery systems we saw were in fabs in the United States.

In cases where a fab scored poorly for certain metrics, the most common reason was that the relevant area was simply not a focus of the fab management. Every participant has certain focus areas that management impresses on the work force as top priorities for improvement; associated with each area is a paradigm for data collection, problem-solving, training, etc., that we call a *religion.* We use the term religion because of the management efforts made to rally the organization around the paradigm, trying to instill belief in the workers that the paradigm will work.

Manufacturing religions we encountered include TQM with its focus on product quality and process control, TPM with its focus on equipment productivity, intensive in-line data collection and statistical analysis of the integrated data, automation for mistake-proofing and productivity improvement, fast cycle time ("time-based competition"), and on-time delivery. These religions are not really exclusive, but many times we observed how a fab, stuck in the paradigms of its religions, simply had not placed any focus on important areas of improvement.

It was fascinating to us to observe the varying strengths of different religions in different parts of the world. TQM was well-established almost everywhere we went. Intensive in-line data collection and statistical analysis of integrated data is strong in at least two thirds of our participants, representing all parts of the globe. TPM is very strong in Japan and in some companies in Taiwan and Korea, but generally weak in the US fabs we visited. On the other hand, cycle time and on-time delivery are strong religions in US and Taiwanese fabs, but generally quite weak in Japanese and Korean fabs. As this is written, no doubt our participants are working to catch up in their areas of weakness.

Since the TPM religion originated in the Japanese machine tool industry, the fact that it has become strong in the Japanese semiconductor industry is perhaps not surprising. What is more surprising is that the cycle time religion, which first flowered in the Japanese automobile industry, flourishes in many American semiconductor fabs we visited yet did not take hold in most Japanese semiconductor fabs we visited. Perhaps the influence of American academia has something to do with it.

With the maturity of TQM and the integrated data analysis religions at most of our participants, defect densities are quite competitive at many of our participants, apart from performance differences associated with process development and transfer. Given the weaker penetration of the TPM religion and of the information handling and step-level automation religion, equipment throughputs and line yields are more prominent discriminators of fab performance in our sample.

The limited penetration of cycle time and on-time delivery religions also ought to discriminate performance in our sample. However, the benefits of cycle time and on-time delivery performance flow primarily to the marketing and financial sides of a company, and unfortunately we are not able to calibrate the participants in those regards.

Checklist of Key Practices

Table S-5 provides a tabulation of particular operational practices, the impacted metrics, and lists of fabs who have taken these actions, roughly ranked by the intensity or effectiveness of practice. As can be seen, the practices are organized into categories labelled CIM and Information Systems, Organizational Practices, Formal Procedures, Process and Technology Improvements, and Production Control.

In the area of CIM and Information Systems, all of our participants have embraced Statistical Process Control (SPC) as a means of detecting manufacturing problems and improving process performance. Almost all provide automated notification of out-of-control conditions. The leading fabs rigorously manage their SPC programs, retiring unneeded control charts and adding new ones recognized as desirable, adjusting control limits as appropriate, adjusting frequencies of measurements to focus efforts on the most critical areas, and maintaining an effective training program. SPC measurements are made both of product wafers and of machine conditions, such as particle counts of machine exhaust flows or of blank wafers passed through the machine. The leading fabs have information systems that automatically provide assistance for responding to out-of-control situations, such as auto-display of corrective action guidelines, automatic disabling of equipment or process, automatic notification of the responsible engineers, etc.

All of our participants have engineering databases to which they upload some amount of metrology data, SPC measurements, and production tracking data (such as which machine was used to process a lot, which operator attended to it, what batch of chemicals was used, etc.). The leading fabs upload more data, and they have automated the upload of much of these data using bar codes, magnetic cards, "smart cards," SECSII interfaces and sensors.

The top fabs efficiently perform end-of-line yield analyses by integrating their engineering database with the database of die yields and parametric measurements taken at the end of the manufacturing line. Automated statistical correlations are made between die yield results and the data uploaded to the engineering database described above, in order to ascertain what characteristics are common to low-yielding wafers. Leading fabs perform extensive analysis of wafer map and bit-fail patterns to find clues to the types of processing equipment where losses were incurred, and they easily carry out ad hoc statistical correlation analyses on the integrated database. The leading fabs document their findings for each major event of yield loss, and save these findings in a database for future reference.

Leading fabs use digital image processing and laser scanning machines to conduct defect inspections of partially-processed wafers. Wafer maps showing the distribution of defects are reviewed. The data is saved in the integrated database for statistical correlation with end-of-line die yields.

The leading fabs make effective use of computers to prevent processing errors. Automated recipe download is installed at most or even all processing equipment in leading fabs. "Smart"

Table S-5
Summary of Effective Manufacturing Practices

Practice	Metrics Influenced	Practicing Fabs
CIM and Information Systems		
SPC	Defect Density, Line Yield	All fabs
Equipment Efficiency Measurement	Equipment Throughput, Cycle Time, Labor Productivity	M4, B3, M6, M3, L8, L14, M10, M2, L6, B5, B4, M9, L8, L1
Visual Displays of SPC Charts, Equipment Tracking, etc.	Line Yield, Defect Density, Labor Productivity, Equipment Throughput	M4, M3, M2
Automation of Data Logging	Cycle Time, Defect Density, Labor Productivity, Equipment Throughput	M4, M6, B3, M3, M2, L6, L1 L8, L13
Auto Recipe Download and/or Display	Line Yield, Cycle Time, Defect Density, Labor Productivity, Equipment Throughput	M6, B3, L6, L4, M4, M2, L1, L3
Automated Feedback Control at Photolithography	Defect Density	M4, B3, L6
Integrated Yield Correlation Analysis	Defect Density	M1, L8, M10, M4, M3, M6, B3, L6, L3, L11, L4, B5, B1
In-Line Electrical Measurements	Defect Density	L6, L4, M4, M3, L11, B5
In-Line Defect Measurements	Defect Density	M1, M10, L6, M3, M4, L4, B3, M6, B1, B5
Automated Trouble Messaging and Automated Assistance for Trouble-shooting	Cycle Time, Line Yield, Equipment Throughput, Labor Productivity	B3, L6

Table S-5 (cont.)
Summary of Effective Manufacturing Practices

Practice	Metrics Influenced	Practicing Fabs
Formal Procedures		
Formal Procedures for New Process Introductions	Defect Density, Line Yield, Equipment Throughput	M1, M4, M6, M10, M3, L14, M2, L13, L15, B3, L4, L6, B1, B5
TPM Program	Equipment Throughput Cycle Time, Line Yield, Defect Density, Labor Productivity	M3, M4, M6, M10, M2, L14,
Organizational Practices		
Exchange of Engineers with Development Fab	Defect Density, Line Yield, Equipment Throughput	M4, M3, M6, M10, M1, L8, B3, L14, L6, B1, L4, B5
Integration of Engineering Groups	Defect Density	M4, M3, B3, M6, L5, M2, L4, L6
Integration of Engineering and Manufacturing Staff	Equipment Throughput, Line Yield, Defect Density	M6, M4, M3, M9, L8, L11
Operator and Technician Improvement Teams	Equipment Throughput, Cycle Time, Line Yield	M3, M4, B3, M2, L1, M6, L11, M9, B6, L16, L8, L4, B5
Mentoring By Senior Engineers and Supervisors	Defect Density, Line Yield Equipment Throughput	M3, M4, M6, B3, M1, M10, L5, L14
Mentoring By Senior Operators	Line Yield, Cycle Time, Equipment Throughput	M3, M4, M6, B3, B5, L4, L8
Extensive Leadership Training	Defect Density, Line Yield, Equipment Throughput	M3, M4, M6
Stretch Goals	Defect Density, Line Yield, Equipment Throughput, Labor Productivity	M4, M3, M6, L6, L4, M10, M1, L16

Table S-5 (cont.)
Summary of Effective Manufacturing Practices

Practice	Metrics Influenced	Practicing Fabs
Process and Technology Improvements:		
Step-Level Automation	Line Yield, Cycle Time, Labor Productivity, Equipment Throughput	L5, M3, M4, B3, M6, M2, L6, B1, B5
Equipment Modifications	Defect Density, Cycle Time, Labor Productivity, Equipment Throughput	M4, M3, L1, B3, L2/M2, M10, L6
Process Flow Re-design	Defect Density, Cycle Time, Line Yield, Equipment Throughput	B5, M3, M4, L14, M1, M10, M2
Product Re-design	Defect Density	B3, M4, M3, M6, M10, M1
Machine Lights and Audio Alarms	Cycle Time, Equipment Throughput, Labor Productivity	M4, M3, B3, M6, L1, L11, M2, M10, L14
Linked Photolithography Cells	Defect Density, Cycle Time, Equipment Throughput,	L1, L11, L8, M4, M2, L5, M6, B3, M9, L6
Automated Interbay Lot Movement	Cycle Time, Labor Productivity	M6, M4, M3, L8, M2, M1, M10, L14
Production Control		
Kanban	Cycle Time, Labor Productivity	B3, L3, L6, M7, L4, B4
Computerized Dispatching	Cycle Time, Labor Productivity, On-Time Delivery	L11, B3, L6, L4, L13, M3, B5, M4
Production Planning Based on Measured Equipment Capacity	On-Time Delivery	B3, B4, B5, L6, M1, M9, L14

lot-machine interfaces have been installed by some leading fabs, whereby the computer system prevents one from tendering the wrong lot or the wrong recipe to the machine. In addition, "smart" lot and reticle racks also are used at one participant that highlight the correct lot and reticle to be used. A couple of leading fabs also have automated the feedback control of photolithography exposures based on critical dimension measurements.

In the area of Organizational Practices, the leading fabs practice considerable integration of sustaining engineering staff with development engineering staff in order to make the introduction of new process flows more successful. The top fabs exchange engineers with the development fab that is the source for their new process flows, sending their own engineers to development before time of transfer, or receiving engineers from development at time of transfer, or both. These steps are taken to ensure the fab has expertise in new process flows right from the moment they enter production, as well as to ensure that new flows and their associated processing equipment are installed, configured and operated to provide the desired results.

The leading fabs have organized the various types of sustaining engineers into more integrated departments of product engineers, process engineers and equipment engineers so as to promote interdisciplinary problem-solving and shared accountability. This integration of what are traditionally distinct engineering groups comes from the recognition that solving yield and throughput problems requires a variety of expertise as well as consideration of many trade-offs, and that specialists in one engineering area will benefit from increased knowledge of related areas. These integrated organizations also feature substantial efforts to mentor technical staff to higher levels of responsibility and higher levels of technical knowledge, e.g., mentorship of junior engineers by senior engineers, mentorship of technicians by engineers, etc.

At leading fabs, improvement projects are not merely the domain of engineers. Improvement teams of operators and technicians are formed and guided by managers and engineers to address and solve manufacturing problems appropriate to their knowledge and experience. This team activity at leading fabs is an essential strategy for training employees and for upgrading their skill and knowledge levels. Umbrella programs such as TQM and TPM are used effectively as a means of rallying and focusing team efforts, and especially for training in formal methodologies for problem-solving. The leading fabs have very large numbers of improvement teams, with nearly every technician and operator involved in improvement projects. Virtually all technicians and even many operators are sent to classes run by equipment vendors in order to increase their equipment knowledge.

The resulting acquisition of skills and knowledge leads to a more productive division of labor in leading fabs. Operators in leading fabs perform preventive maintenance and minor repairs of processing equipment, help design SPC charts, and participate in trouble-shooting efforts following formal methodologies. Technicians are thus freed to put more focus on on major maintenance and repairs, improvement projects, training, and the documentation of equipment-related procedures. In turn, engineers leverage these resources to increase their rate of progress on both long-term improvement projects and more short-term trouble-shooting efforts.

The leading fabs engage in extensive mentorship and employee development at all levels, with senior managers developing managers, senior engineers developing the engineers working with them, right down to senior operators and technicians developing operators in each equipment bay. In lieu of hiring professional supervisors, leading fabs promote experienced line

workers to positions as group leaders, where their knowledge and experience makes them suitable to serve as mentors to workers in their area. At these fabs, there is extensive and continuing leadership training for engineering and manufacturing managers, all the way up to the executive officers.

Not only do the leading fabs establish programs for continuous improvement, they also set ambitious stretch goals for improvements in productivity and quality that force systemic improvements, and they do extensive technical planning, project and team planning and mentoring to realize those goals.

In the area of Formal Procedures, the leading fabs have established formal procedures governing the transfer and introduction of new process flows. There also are efforts at leading fabs to modularize process design, whereby new processes make use of proven modules from previous-generation processes, where feasible to do so. Such procedures serve to maximize the likelihood that new processes provide favorable yields in the first quarter of production, and that volume may be ramped quickly.

While all of our participants use SPC as a formal procedure for in-line measurement of quality, and all of our participants make efforts to measure equipment availability and utilization, the leading fabs have formal procedures for the measurement of overall equipment efficiency rather than merely its availability. The leading fabs also have formalized the improvement of procedures for equipment maintenance, operation, analysis and training under the TPM paradigm.

In the area of Process and Technology Improvements, the leading fabs make useful modifications to processing equipment to reduce downtime, to reduce particles, to reduce wafer breakage or scratches, to reduce handling, to reduce machine setups, to reduce the need to process test or pilot wafers, and to reduce unit processing times. They have the necessary expertise on-site, they obtain support from equipment vendors as required, and they have an organizational structure that integrates process and equipment engineers so as to deduce the most prudent equipment modifications to make considering the desired process characteristics. The leading fabs have installed lights and audio alarms on the processing machines to focus attention on idle or malfunctioning machines. Photolithography at the leading fabs is performed in linked cells achieving superior die yields, low rates of rework, low cycle times and high throughput.

Sometimes, modifying the equipment is not the most effective solution to a yield problem. The leading fabs also make changes to product designs or process flows for increased manufacturability. Such changes reflect an organizational structure that integrates product, process and equipment engineers, enabling them to identify and make trade-offs between potential equipment and product changes.

Special mention should be made of the application of standard mechanical interface (SMIF) technology, involving the implementation of micro-environments for processing equipment and lots. We have seen one participant, using an older and much more modest clean room than other participants operating comparable process flows, obtain world-class defect densities. The introduction of SMIF technology clearly extended the economic life of this older fab and thus constitutes a very good technological improvement. The isolation of each machine from the rest of the fab also facilitated staged and selective upgrading of the equipment set in the fab.

Special mention also should be made with respect to the leading fab in terms of cycle time. Over several years, this fab has steadily re-arranged its layout to break up the standard farm-type layout in favor of smaller cells of equipment handling a smaller variety of operation sequences. While in the past cell-type layouts have been resisted by many fab designers for fear of lost equipment utilization, this same fab is also our leader in 5X stepper throughput. This fab has demonstrated that a more cell-type layout represents a technological improvement, in that cycle times can be reduced while achieving leading-edge equipment throughput.

Finally, in the area of production control, the leading fabs perform automated production planning based on measured equipment capacity and cycle times to achieve high levels of on-time delivery. Re-planning is performed frequently and swiftly to keep up with revised intelligence on market demand and customer orders. On the factory floor, both Kanban and computer-assisted dispatching (lot sequencing) are used by leading fabs to improve cycle time as well as on-time delivery.

Plans for the Continuing Survey

The Competitive Semiconductor Manufacturing program was chartered as a multi-year research effort with the goal of measuring and analyzing the performance of 25-30 wafer fabs. We have studied three fabs in a Pilot Phase and twenty eight fabs in the Main Phase over the first 5 years of this program. We have identified relationships between values of performance metrics and manufacturing practices, as summarized above.

Our funds received from the Sloan Foundation will be exhausted before the end of 1996. We hope to continue our Main Phase competitive studies of semiconductor manufacturing with industry sponsorship. We have received modest support from Sematech, EAIJ and SIRIJ, and we will be soliciting further industry support during the second half of 1996. We also will solicit additional funding from the Sloan Foundation for PhD student and faculty research concerning semiconductor manufacturing in two areas: (1) the integration of product design, process development and transfer to mass production, and (2) enhancing factory throughput through automation, equipment efficiency improvement and yield analysis.

1. Introduction
by Robert C. Leachman

This document presents the results of the first three and one half years of the Main Phase of the Competitive Semiconductor Manufacturing (CSM) survey, a multi-year research program to study competitive semiconductor manufacturing worldwide. The study is a joint project of the College of Engineering, the Haas School of Business, the Institute of Industrial Relations and the Berkeley Roundtable on the International Economy at the University of California at Berkeley, under sponsorship of the Alfred P. Sloan Foundation, and with the cooperation of leading semiconductor producers from Asia, Europe and the United States. Professors David A. Hodges and Robert C. Leachman are the project's Co-Directors.

U.C. Berkeley researchers performing this study are faculty, senior research staff and graduate students from Engineering, Business School and Economics. Many of the participating firms are also represented on the project's Industry Advisory Board, which has played an important role in refining the research agenda. Appendix A of this report contains a complete list of all researchers participating in the Main Phase and a list of the Advisory Board members. The firms participating in the CSM Survey to date are listed in Table S-1.

The CSM program includes in-depth studies of specific issues in addition to the field survey studies described in this report. Comments and suggestions from those in industry and the academic community interested in the measurement, understanding and improvement of manufacturing performance in this industry are always welcome.

The CSM survey has three major tasks:

(1) To measure and compare the manufacturing performance of the semiconductor industry's major producers;

(2) To identify and account for the observed variations in performance -- what is the range of performance of various plants (while preserving confidentiality as to identity of specific plants), and why do some plants do well while others do not as well; and

(3) To document and describe the competitive, 'best-of-breed' manufacturing practices that deliver world-class manufacturing performance.

At the outset of the CSM survey, it was decided to bound its scope to tractable proportions. Rather than attempt to address overall industry competitiveness, the focus of this study is the contribution of *manufacturing* performance to competitiveness. World-class manufacturing is an obvious contributor to competitiveness, but, for reasons that may include inferior designs, architectural dominance, trade barriers, and short time horizons, even world class manufacturing may be no guarantee of competitive success. Secondly, we decided to limit the scope of the study of manufacturing competitiveness to the so-called "front end" of the overall semiconductor manufacturing process, i.e., wafer fabrication ("wafer fab") and wafer electrical test ("wafer probe") facilities that turn blank silicon wafers into completed wafers with functioning electrical circuits on them. Time and resource constraints prevent us from analyzing the entire manufacturing flow in numerous companies; since differences in performance are thought to be most significant in wafer fab, we have omitted competitive analysis of device packaging and final test manufacturing processes.

Before starting the Main Phase of this survey, the study team undertook a Pilot Phase study -- an effort on the researchers' part to refine the study methodology, to identify the level of investigation that was manageable given the time and budget constraints, and to learn by doing. The Pilot Phase transpired during the Fall of 1991. Three companies with long-term ties to U. C. Berkeley - NEC, Hewlett Packard, and Intel - participated in the Pilot Phase; the results of this phase are described in a research report released in the spring of 1992. [2]

As a result of our experience in the Pilot Phase, we formulated a strategy for measuring front-end manufacturing performance and for identifying the practices that best explain differences in performance, summarized as follows. First, a Mail-Out Questionnaire (MOQ) is sent to each participant. This questionnaire requests objective technical data such as clean room dimensions and cleanliness class; major fab process flows in production over the last four years; historical equipment counts and head counts; historical wafer start volumes in each process flow, and consequent line yields, die yields and cycle times; major computer hardware and software systems in use, material handling automation in use, human resources data, etc. As the Main Phase progressed, we made several refinements and additions to the MOQ. From an initial length of about 50 pages, the MOQ has subsequently grown to its current length of 100 pages. Our participating fab lines report that the MOQ requires between 80 and 160 man-hours to complete.

From the answers supplied by the participants to this questionnaire, we developed various manufacturing efficiency measures such as line yield, defect density, equipment productivity, labor productivity, etc. Chapter 2 of this report summarizes such measurements of the first twenty eight participants in the Main Phase of the CSM Study. Questionnaires from these participants were received during the period June, 1992 until October, 1995; thus the starting points and ending points for metric scores vary among the participants. For several of our early participants, an additional two years of MOQ data was requested and received. Indicative of the pace of change in the industry, three of the fab lines we studied have now been closed, three have increased their wafer size, and one other has been sold.

We observed wide variations of performance for each of the performance metrics. From the MOQ performance data it is possible to rank the participants for each of the metrics, but it is not possible to discern why the participants achieved disparate performances. For this latter purpose, we followed up the receipt of each completed questionnaire with a two-day Site Visit by a 6-9 person research team of faculty and graduate students. All twenty eight of the participants in the Main Phase hosted a two-day Site Visit by our study team sometime during the period June, 1992 - December, 1995. During the Site Visit, a tour of the fab is made, a series of interviews of a cross-section of the organization (managers, engineers, technicians, operators) is made, and a series of sessions is held discussing the fab's approach to various improvement problems (yield improvement, productivity improvement, cycle time reduction, equipment efficiency improvement, on-time delivery improvement, managing the introduction of new process flows) and improvement techniques (process control, computer-intergrated manufacturing and information systems, work groups and problem solving teams, human resources development, cost accounting

2. See *The Competitive Semiconductor Manufacturing Survey: Results of the Pilot Phase,* by Michael Borrus and Robert C. Leachman, Report CSM-01, Engineering Systems Research Center, University of California at Berkeley, Berkeley, CA 94720 (May, 1992).

practices, and managing relations with suppliers and vendors). From these more qualitative data would emerge a picture of the fab's manufacturing practices which could be correlated with its performance.

Chapter 3 of this report discusses our findings in this regard for the twenty eight participants of the Main Phase. We describe our findings in some detail concerning the managerial, organizational, information system and human resource practices that seem to underlie performance at the participants.

Our major explanatory variables focused on differences in the process and technology improvements undertaken, organization and management systems, people skills and activities, and the use of information technology. Again we encountered surprisingly wide variety among the participants in each of these practices. Companies achieved good results in different ways and poor results for varying reasons. Despite that variation, it is possible to identify a set of practices characteristic of those fabs achieving high scores in our manufacturing metrics. These practices are summarized in the Executive Summary, shaping a set of manufacturing practices that underlie world-class manufacturing performance.

Finally, Chapter 4 outlines our plans for further progress and refinements of our approach in the Main Phase of the CSM survey.

This report is the third we have issued concerning findings in the Main Phase of the CSM survey. Our first report on this subject, released in the spring of 1993, summarized our findings concerning the first eight participants in the Main Phase. [3] Our second report, released in the summer of 1994, summarized our findings concerning the first sixteen participants in the Main Phase. [4] This report extends our previous reports, as we provide herein our findings concerning the first twenty eight fabs in the Main Phase.

Two caveats are in order before proceeding. First, we estimate that there are perhaps 1,200 semiconductor wafer fabrication facilities in operation throughout the world; our paltry sample of 28 fab lines certainly can not be viewed as statistically representative. Most of the fabs in our survey were constructed in the middle or late 1980s or early 1990s; practices and performance at older fab lines or at newer fab lines may be considerably different.

Second, our participants serve a diverse set of markets -- commodity memory devices, standard logic, ASIC (application-specific integrated circuits), foundry services, and captive production for a parent computer manufacturer. In these various business, the various performance metrics have varying importance. Moreover, the equipment and process technology in use varies by type of device produced, and different equipment and technologies are capable of quite different performance. For these reasons, we have divided the presentation of measurements into three categories, still quite broad in scope: memory fabs, CMOS logic fabs, and medium-scale integration (MSI) fabs. Memory fabs use submicron CMOS technology to produce advanced

3. See *The Competitive Semiconductor Manufacturing Survey: First Report on Results of the Main Phase,* Robert C. Leachman (ed.), Report CSM-02, Engineering Systems Research Center, University of California at Berkeley, Berkeley, CA 94720 (April, 1993).

4. See *The Competitive Semiconductor Manufacturing Survey: Second Report on Results of the Main Phase,* Robert C. Leachman (ed.), Report CSM-08, Engineering Systems Research Center, University of California at Berkeley, Berkeley, CA 94720 (August, 1994).

memory devices such as 16M DRAMs, 4M DRAMs and 1M SRAMs. CMOS logic fabs also use CMOS technology to produce advanced logic devices such as microprocessors and microcontrollers with feature sizes smaller than 1.5 microns. MSI fabs use older process technologies including Bipolar, BiCMOS and 1.5 - 4.0 micron CMOS to produce a variety of logic, signal processing and power devices. The memory fab category includes 10 fab lines, the CMOS logic fab category includes 16 fab lines, while the MSI fab category includes 8 fab lines. In some cases, we have classified a participant into more than one category. Four participating fabs appear in both the memory and CMOS logic categories, while one other fab appears in both the CMOS logic and MSI fab categories.

Third, under the terms of our agreements with the participants in this survey, we protect the confidentiality of their manufacturing data. We have provided statistics for the twenty eight participating fabs, but with identities masked using the labels M1, M2, M3, $\cdots$, M10 for memory fab lines, the labels L1, L2, L3, $\cdots$, L16 for CMOS logic fab lines, and the labels B1, B2, B3, $\cdots$, B8 for MSI fab lines. Each participating fab is consistently identified using the same labels in all tables and graphs of scores for the various metrics. We have sometimes masked the discussion of manufacturing practices even further, using different labelling schemes for participants or by simply classifying particular practices only as to whether they are exhibited by top, intermediate or low performers (in terms of metric scores.) In this way, the range of metric scores and practices encountered may be discussed without revealing the particular identity of which fab achieved which scores using what practices.

2. Factory Performance Measurements
by Robert C. Leachman

Wafer fab technical efficiency may be studied in terms of components for yield, equipment productivity, labor productivity, and manufacturing cycle time. We present ten such metrics of technical efficiency computed for the survey participants over time. Additional technical metrics concerning equipment maintenance are presented in section 3.4 of Chapter 3. Not every metric could be computed for all participating fabs, as some metrics do not apply to all fabs, and some fabs were not willing and/or not able to supply all the data requested in the Mail-Out Questionnaire.

The technical metrics include the following:

- line yield per twenty mask layers;
- defect density (normalized die yield);
- integrated yield (combining line yield and normalized die yield);
- 5X stepper throughput (total 5X exposure layers completed per 5X stepper per day);
- ion implanter throughput (total implant layers completed per ion implanter per day);
- metallization machine throughput (total metal layers completed per metallization machine per day);
- integrated 5X stepper throughput (combining integrated yield and stepper throughput);
- cycle time per mask layer;
- direct labor productivity (total mask layers completed per operator per day); and
- total labor productivity (total mask layers completed per total head count per day).

Each of these metrics is formally defined and explained below, but beforehand, it is useful to describe the variety of characteristics of the twenty eight participating fabs. As a matter of terminology, a *process flow* defines a family of products produced according to the same series of fab processing steps. Typically, the only difference among several products belonging to the same process flow is the particular masks used at photolithography steps. [5] Thus for all fab equipment types except photolithography exposure machines, the breadth of product mix is commonly characterized in terms of the breadth of process mix. For photo exposure machines, product mix is characterized by the number of different die types that are in production.

Tables 2.1 - 2.3 display the characteristics of the participating fabs, sorted into categories for production of submicron memory products, CMOS logic products with feature sizes smaller than 1.5 microns, and medium-scale integration (MSI) products. The tables indicate total wafer starts per week, the number of different process flows in operation, the types of products produced, the number of active die types, the equipment type most heavily loaded in the fab, and a qualitative index of how heavily the fab was loaded compared to capacity. The figures shown are the most recent ones made available for our survey; wafer start figures are rough averages of the

5. This is the case in CMOS process flows. In bipolar or analog process flows, different products in the same flow may have slightly different machine settings at the same process step, as it may be necessary to "tweak" the process for different products in order to provide favorable yields.

Table 2.1. Characteristics of Participating Memory Fabs

Fab ID	Wafer size (mm)	Wafer starts per week	No. of major process flows	No. of active die types	Major products	Bottle-neck eqpt. type	Factory workload vs. capy
M1	150	5,400	1	6	4M DRAM	PE	H
M2	150	10,000	4	80	4M DRAM	S	H
M3	150	15,000	55	320	4M DRAM, 1M SRAM, EEPROM, Mask ROM	S	H
M4	150	12,000	3	12	4M DRAM, 1M SRAM	S	H
M5	150	7,800	3	40	1M SRAM	S	H
M6	150	8,000	3	15	4M DRAM, 16M DRAM	S/Imp	H
M7	150	2,000	9	85	256K SRAM, EEPROM	Dif	H
M8	150	7,200	3	140	1M SRAM	S	H
M9	150	1,200	2	3	1M SRAM	S	H
M10	150	13,000	7	10	4M DRAM, 1M SRAM, Mask ROM	S	H

Abbreviations: PE - plasma etch, S - 5X stepper, Imp - high current ion implant, Dif - diffusion furnaces, H - high, M - medium, L - low.

Table 2.2. Characteristics of Participating CMOS Logic Fabs

Fab ID	Wafer size (mm)	Wafer starts per week	No. of major process flows	No. of active die types	Major products	Bottle-neck eqpt. type	Factory workload vs, capy
L1	125	4,800	5	85	ASIC	Met	H
L2	150	10,000	4	80	MPU, MCU	S	H
L3	150	600	2	13	MPU	Met	H
L4	150	3,000	4	50	MPU, MCU	S	H
L5	150	7,800	3	40	MPU, MCU	S	H
L6	125	5,500	12	200	MPU	S	M
L7	125	3,300	10	400	Embedded DSP	CVD	H->M
L8	150	4,500	1	5	MPU	S	H
L9	150	15,000	55	320	ASIC, MPU	S	H
L10	125	300	2	10	MPU, MCU	Dif	L
L11	150	1,900	7	600	ASIC	S	M
L12	150	2,000	9	85	MPU	Dif	H
L13	125	4,200	5	150	ASIC	Dif	H
L14	150	7,200	3	140	MPU, MCU	S	H
L15	150	2,500	3	15	ASIC	S	H
L16	125	6,600	3	50	MCU	S	H

Abbreviations: Met - metallization, CVD - chemical vapor deposition, S - 5X stepper, Dif - diffusion furnaces, H - high, M - medium, L - low.

Table 2.3. Characteristics of Participating MSI Fabs

Fab ID	Wafer size (mm)	Wafer starts per week	Number of major process flows	Number of active die types	Major products	Bottle-neck eqpt. type	Factory workload vs. capy
B1	125	2,800	3	65	Power, ASIC, Signal processing	C	M
B2	125	3,300	10	400	Embedded DSP	CVD	H->L
B3	100->125	11,000	6	180	Bipolar logic	S	M->H
B4	125->150	900	4	61	Power, CMOS MPU, Signal Processing	C	M
B5	100	1,800	3	45	Bipolar & CMOS MCU, Signal processing	C	H
B6	125	2,600	10	212	Bipolar logic	PE	L
B7	150	2,000	5	200	Power, Analog	PA	H
B8	100	11,000	5	130	Power, Analog	PA	H

Abbreviations: C - coat and develop tracks, CVD - chemical vapor deposition, S - 5X stepper, PE - plasma etch, PA - projection aligner, H - high, M - medium, L - low.

wafer starts per week for the most recent quarter recorded by the participant, generally some time between mid-1992 and mid-1995. As can be seen, weekly wafer starts range from a low of 300 to a high of about 15,000, a factor-of-fifty range. The number of fab process flows ranges from only one up to 55, also a factor-of-fifty range. Note that volume and mix are not correlated in our sample; for example, fab L8 has moderately high volume, but an extremely narrow product/process mix; fab M6/L9 has the highest volume but also an extremely broad process mix; fab L11 has relatively low volume but a very high number of die types, etc.

The 5X steppers are the most common fab bottleneck, but other equipment types show up as well. All memory fabs and most CMOS logic fabs are heavily loaded, but a number of the MSI fabs have a relatively low workload, perhaps reflecting their nearing end-of-life status.

Figures 2.1 - 2.41 and Tables 2.4 - 2.42 placed at the end of this chapter present metric scores for the participants. Before discussing these scores, we formally define the metrics themselves.

2.1 Yield Metrics

Line yield expresses the average fraction of wafers started that emerge from the fab process flow as completed wafers. Wafers may be unintentionally broken or scratched during processing due to handling mechanism malfunctions or operator mishandling. Line yield losses also result from processing cycles that are aborted due to equipment malfunction, and from wafers rejected by quality inspections that detect misprocessing. Misprocessing can result from human errors (wrong recipe selected, processing step repeated or skipped, etc.) as well as from out-of-control process conditions. Thus line yield scores reflect the level of equipment reliability, the degree of process control, and the level of operator proficiency. They also may reflect the degree of focus in the factory, since a factory operating a single process flow needs to make far fewer adjustments of the equipment than one operating multiple process flows.

All other factors being equal, line yields tend to be higher in large fabs with a low number of process flows, whereby processing equipment may be dedicated to performing a single process recipe. In all fabs, improvements in line yields can result from the introduction of more sophisticated process control, the automation of recipe download, the introduction of controls preventing the processing of the wrong lot, improvements to equipment reliability, and from increasing operator understanding of processing procedures and trouble-shooting instructions. Of course, higher line yields reflect more useful output per unit input and thus higher productivity.

The number of circuitry layers varies according to the complexity of the product. All things being equal, one would expect the line yield for a product with more layers to be lower. Thus we normalize our line yield measurements to be expressed in terms of line yield per twenty layers of circuitry. That is, the given line yield for a process flow is converted into a metric score for the line yield per twenty layers using the following formula:

$$LY20 = LY^{(20/ML)}, \tag{1}$$

where ML is the number of mask layers in the process flow, LY is the reported line yield for the process flow, and $LY20$ is the calculated line yield per twenty layers.

We computed the line yield per twenty layers for each major process flow (up to a maximum of four flows for each participating fab) by quarter going back several years, and then summarized the scores up to the fab level by computing a weighted average line yield for the entire fab. The weights used were the number of wafer starts in each process flow.

Rarely does every integrated circuit printed on a completed wafer function properly. Following completion of the fab process flow, wafers are electrically tested in an operation known as "wafer probe" or "die sort". Each integrated circuit ("die") on the wafer is tested ("probed") to see if it functions, and inoperative die are identified to be discarded later. The fraction of the total die on a wafer that pass the wafer probe test is termed the *die yield* of the wafer. Typically, die yield accounts for a larger loss of potential output than does line yield. [6]

Causes of die yield losses may be classified into (1) *large-area faults,* and (2) losses due to contaminating particles lodged in the circuitry, the latter often referred to as simply *defects.* Large-area faults arise from a failure of the processing equipment to correctly perform the desired process operation (e.g, over-etching, excessive or inadequate deposition of dopants, lack of registration of photo layers, etc.). These faults typically show up as wholesale or patterned areas of the wafer surface with few or no dice performing as desired, or as entire wafers or even entire lots of wafers with no working dice. On the other hand, particles are much smaller than the area of a die; a single particle may cause the circuit to have a short or an open, thereby causing the die to fail. Thus defects can lead to randomly distributed patterns of failed die over the wafer surface.

Following the life cycle of a typical CMOS process flow, failed-process problems are usually driven out early in the life of the flow as process and equipment control are improved and/or as the products are re-designed to better conform with the capabilities of the equipment. Occasionally, failed-process problems may persist if a fab deliberately utilizes low-cost, older-generation processing equipment that is marginally capable of performing the desired process, and/or if the product design deliberately violates one or more "design rules" governing the process. Apart from such cases, failed-process problems tend to be an early-life issue, and die yield losses in mature CMOS process flows tend to be dominated by particle losses.

Historically, people and the ambient clean room air were thought to be the primary sources of contaminating particles, but as clean room air flow and wafer protection have been improved, it is now generally believed that 80% or more of fatal defects land on the wafers while they are resident in the processing chambers of the fab equipment. Pressure spikes in processing chambers, leaks in vacuum chambers during evacuation, flakes given off by handling mechanisms, air bubbles in photoresist applications, contaminated liquid and gas flows, etc. are examples of particle problems. Thus overcoming particle losses also is an equipment improvement issue.

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6. A caveat is in order concerning the line yield and die yield metrics. (The latter yield is measured in terms of a defect density metric discussed below.) There is some potential for trade-off between line yield and die yield. For example, one might increase in-line wafer inspections in order to detect processing problems before lots reach wafer probe, scrapping those wafers failing the inspections. As another example, the rules for lot disposition following an undesired processing event may be more restrictive at some fabs than others (e.g., if a wafer breaks in a processing chamber, one fab might scrap all other wafers in the chamber while another might simply clean the other wafers and continue processing them). In such cases, there may be some sacrifice of line yield in exchange for the opportunity to increase die yields and/or increase product reliability.

While particle-related losses have been theoretically modelled as randomly distributed over the wafer surface, equipment operating improperly or with improper controls may spew out dense bursts of particles (sometimes characterized by certain "signature" patterns on the wafer), causing the die populating a large portion of the wafer to fail. In general, defects are not distributed uniformly over the surface of a wafer, nor are they distributed uniformly from wafer to wafer.

Thus it is not easy for the participants to precisely sort out die yield losses by process-failure and particle causes, as the pattern of failed die on a wafer could have resulted from many combinations of causes. The die yields reported by the participants are simply the observed yields at wafer probe, reflecting both particle-related losses and large-area faults.

Although particle-related losses do not fully account for total die yield losses, they are nonetheless significant, and everything else held equal, a product with a larger die size may be expected to have a lower yield, since it has a higher probability of hosting a fatal particle. Thus to compare die yields among participants, one needs to normalize for die area. In this report we normalize die yields reported by the participants to account for differences in die size, making use of a *defect density* metric that expresses the number of fatal defects per square centimeter of wafer surface area. We use the basic Murphy defect model to convert actual die yield recorded for a major product in each process flow into a defect density score for the process flow. Specifically, this model expresses the fractional die yield (i.e., the fraction of gross die that pass the electrical tests at wafer probe) as

$$Y = \left[\frac{1 - e^{-AD}}{AD} \right]^2, \qquad (2)$$

where Y is the observed die yield, D is the defect density over the wafer surface and A is the die area in square centimeters. We use this basic Murphy model below to report trends in defect densities for the participants, whereby trends in die yields for the major products produced in each major fab process flow are converted into trends in defect density using this formula. Although the Murphy model and other defect density formulas were designed as a means of analyzing particle-related losses, in this report we use the defect density metric as a normalized measurement of *total* die yield loss.

When calibrated on the yield of a high-volume wafer type produced at high yields (say, greater than 60%) in a given CMOS fab process, this formula has proved to be fairly accurate in predicting die yields of other product types produced in the same fab process flow. Low die yields (equivalently, high defect densities) suggest that parametric problems probably dominate particle-related defects, and in such cases, "defect density" is a misnomer; in any case, it is an oversimplification.

As fabs introduce process flows for fabricating circuits with finer and finer geometries, particles with smaller and smaller sizes can be fatal. Thus an improved level of particle control is necessary to achieve the same die yield for a finer geometry, and accordingly, process flows need to be classified by geometry for comparison of defect densities.

A further classification that is necessary is to segregate process flows for making logic devices from those for making memory devices. This is because of the substantial amount of

redundancy built into memory circuits, whereby failed memory cells can be disconnected and replaced with spare cells included in the product design for this purpose. (This operation, known as "laser repair," is performed using lasers at the wafer probe operation.) For memory devices, the final die yield is called the "repaired yield," while the die yield before the laser repair operation is called the "virgin yield". Since most of our participants provide us with the repaired yield but not the virgin yield for their memory devices, our participants have requested that we segregate the metric scores for memory and logic flows.

To compare die yields of the different participants, we sort process flows into CMOS logic, CMOS memory, and Bipolar categories, further categorized by the minimum geometry achievable with the flow. We have defined defect density categories for 0.45 - 0.6 micron CMOS memory, 0.7 - 0.9 micron CMOS memory, 0.7 - 0.9 micron CMOS logic, 1.0 - 1.2 micron CMOS logic, 1.3 - 1.5 micron CMOS logic, 1.5 - 4.0 micron CMOS and BiCMOS process flows, 1.2 - 3.5 micron Bipolar process flows, and 5.0 -10.0 micron Bipolar process flows. [7]

To obtain overall front-end yield scores for the participants, we define an *integrated yield* metric as follows. For each process flow of each participant, the defect density score D derived using (2) from the participant's given die yield is plugged back into equation (2) along with a die area $A = 0.5$ sq cm to estimate a die yield Y the flow would achieve if it were producing a product with a die area of 0.5 sq cm. This die yield is then multiplied by the fab-level line yield score $LY20$ computed using (1). Mathematically, we write

$$IY = (LY20)\left[\frac{1 - e^{-(0.5)D}}{(0.5)D}\right]^2, \tag{3}$$

where D is the calculated defect density for the process flow, $LY20$ is the calculated line yield metric for the fab, and IY is the resulting integrated yield for the process flow. This integrated yield metric is reported in the same process categories as described above for the defect density metric.

2.2 Equipment Productivity Metrics

Photolithography typically comprises the highest concentration of capital expense of all equipment types in a wafer fab and is most commonly the long-run equipment bottleneck. Thus the measurement of photolithography equipment productivity is sometimes used as a proxy for measuring the wafer throughput efficiency of a fab.

Although photolithography usually represents the greatest concentration of capital expense for equipment in a fab, 5X steppers are not the bottleneck equipment type in some of the participating fabs, as indicated in Tables 2.1 - 2.3. Even when the equipment set installed in the fab was sized with the expectation that photolithography would be the capacity limiter, changes in

7. Only one of our participants to date operates process flows in the 0.5 - 0.6 micron CMOS logic category, and only two provided data on flows in the 1.0 - 1.2 micron CMOS memory category. These categories have been omitted from this report, since the number of such flows in our sample is too small to report the results and still protect the confidentiality of our participants.

machine rates, setup requirements, and/or in demand mix since fab start-up may have shifted the bottleneck away from photolithography. Thus limits on the utilization of 5X steppers at some participants may be imposed by a lack of capacity available at other equipment types, considering the demand mix.

While equipment performance is commonly measured in terms of percentage equipment utilization, we eschew such a measure here. This is because many of our participants are able to engineer significant reductions in reticle (mask) setup and wafer processing times, and such productivity gains are not measurable with a simple utilization metric. Since equipment throughput may be increased not only by increasing equipment availability and utilization but also by reducing mask setup and wafer processing times, it is necessary that a metric be devised that measures true wafer throughput of the equipment. Ideally, an overall equipment efficiency metric, such as proposed under the Total Productive Maintenance (TPM) paradigm should be used. [8] Unfortunately, such a metric requires a specification of the processing times for the products of the participants, which is beyond our data resources. A simpler measure of wafer throughput is therefore proposed, explained as follows.

The various types of photolithography equipment (pre-bake ovens, coat tracks, exposure machines, develop tracks, inspect stations, etc.) are operated in sequence to perform the photolithography process, whereby the exposure machine is generally the slowest and most expensive. The exposure machines in use at most of our participants are known as "5X steppers". "Steppers" derive their name from the way they work. To expose circuitry patterns in submicron geometries with sharp focus, it is not optically feasible to expose an entire wafer at once. Instead, small groups of die are exposed in sequence, whereby the machine "steps" over the wafer surface making multiple exposures in order to expose all of the die on the wafer. [9]

The total time for a stepper to process a wafer is a complex function of the field size the stepper is configured to expose, the number of die that fit into a field, the number of die on the wafer, and the exposure durations required at various layers. Exposures for metal layers take longer than for other layers. Thus there is variation in the total amount of stepper processing time embodied in each product, and one might expect, say, a plus or minus 15 per cent variation in wafer throughput for 5X steppers operated with the same efficiency under different product mixes.

Some of our participants have argued that stepper scores need to be conditioned based on the number of mask changes that are necessary, i.e., based on the variety of die types that are produced. A machine "setup" involves a particular mask to be used that must be inserted in the machine, and, in some fabs, tested before allowing repetitive use. While a stepper may accommodate up to a dozen or so masks in its magazine, it is nevertheless argued that a fab that must process hundreds of die types per day will of necessity experience more lost stepper time than another fab producing only a handful of die types.

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8. See, for example, *Introduction to TPM*, S. Nakijima, Productivity Press, Inc., Cambridge, MA, 1988.
9. Older processes with minimum feature sizes above one micron can make use of 1X steppers or "projection aligner" exposure machines, the latter of which expose an entire wafer at once. Some participants "mix and match" the use of steppers for critical layers and the use of aligners or 1X steppers for noncritical layers, even for submicron geometries. There are also several generations of 5X steppers with varying accuracy and varying cost; many fabs mix and match different generations of steppers.

However, we have observed fabs in which the requirement to do test exposures following a mask change has been eliminated, and whereby mask changes themselves have been mostly or fully automated. Setups in these fabs require something on the order of 30-45 seconds, rather than the 15-20 minutes or more consumed in many fabs. Indeed, some of the participants with the highest stepper scores discussed below have very high active die counts in their fab. Thus we make no modification for product mix in measuring stepper throughput, and we view all time spent on setups as efficiency loss that potentially can be engineered out.

We define the *stepper throughput* metric as the average number of wafer operations performed per machine per calendar day, considering only mask layers exposed using 5X stepper (photolithography) machines in the numerator and considering only the number of 5X stepper machines installed in the fab in the denominator. This metric is computed at the fab level by quarter going back several years. Although the exact number of wafer operations actually performed at photolithography is not requested in our Mail-Out Questionnaire, we estimate the number of wafer operations SWO performed on 5X steppers for each process flow as

$$SWO = (WS / 7) (NS) (LY'), \tag{4}$$

where WS is the average number of wafer starts per week for the process flow divided by 7 calendar days per week, NS the number of mask layers in the process flow performed on 5X steppers, and LY' is an inflated line yield given by

$$LY' = (1.0 + LY)/2, \tag{5}$$

where LY is the reported line yield for the process flow. (This inflated line yield allows for half of the total line yield loss to load photolithography, or equivalently, the average wafer that is scrapped makes it through exactly half of the layers before being discarded.) Considering all process flows, the total stepper operations per day is summed up, then divided by the number of 5X steppers in service to obtain the value of the metric.

For fabs producing 4 inch or 5 inch wafers, conversion factors have been applied to convert raw scores into 6-inch equivalent scores. To make this conversion, we assumed a standard processing time per six-inch wafer that consists of a fixed component of 40 seconds to exchange wafers and align, plus 80 seconds to step through the exposures of the wafer, for a total of 120.00 seconds. Standard processing times for other wafer sizes include the same fixed component for wafer exchange and align, but with the exposure time component adjusted in proportion to the change in wafer surface area. Thus standard processing time for a 5-inch wafer is assumed to be 95.56 seconds, and for a 4-inch wafer it is assumed to be 75.56 seconds. The ratios of such standard times serve for converting 4-inch and 5-inch wafer operations per day into equivalent 6-inch wafer operations per day.

The most expensive machines per unit used in wafer fabrication are ion implanters. Ion implant machines are not required to process every layer of circuitry, and so the total capital investment in implanters in most of our participants is not as high as the investment in

photolithography equipment. However, given its high unit cost and very large space requirement, ion implant is sometimes the fab bottleneck, and productivity of these machines is important in any case.

Our participants employ three varieties of ion implant machines. Medium current machines perform relatively light-dosage implant operations, processing one wafer at a time. High current machines perform high-dosage implant operations, processing an array of 13 up to 25 wafers at the same time, depending on wafer size. Flexible-current machines also process an array of wafers simultaneously, performing both light-dosage and high-dosage operations. The processing time depends on the dose, the implant beam energy, the implant species (Boron, Phosphorous, Arsenic, Antominy, etc.) and the type of implanter used. Every process flow among our participants includes a mix of medium-current and high-current implant operations, although the mix and nature of the operations varies according to the product design. Given the limited detail of the MOQ data, our overall implanter productivity metric is of necessity highly aggregate and approximate.

Similar to the stepper throughput metric, an ion implanter throughput metric has been defined as follows. We define the *implanter throughput* metric as the average number of implant layers completed per machine per calendar day, considering the completed number of implant layers in the process flows of the fab in the numerator and considering the total number of high, medium and flexible current ion implant machines installed in the fab in the denominator. This metric is computed at the fab level by quarter going back several years. In some cases, some of our participants may have two implant operations in the same implant layer of a process flow; thus our metric for the number of implant layers completed is sometimes less than the number of implant operations actually performed. Although the exact number of implant layers completed per day is not requested in our Mail-Out Questionnaire, we estimate this number IWO for each process flow as

$$IWO = (WS / 7) (NI) (LY'), \tag{6}$$

where WS is the average number of wafer starts per week for the process flow divided by 7 calendar days per week, NI the number of implant layers in the process flow, and LY' is the inflated line yield given by (5). (As before, this inflated line yield allows for half of the total line yield loss to load ion implant, or equivalently, the average wafer that is scrapped makes it through exactly half of the implant operations before being discarded.) Considering all process flows, the total implant operations per day is computed, then divided by the number of ion implanters in service to obtain the value of the metric.

For fabs producing 4 inch or 5 inch wafers, conversion factors have been applied to convert raw scores into 6-inch equivalent scores. To make this conversion, we observed that the load size on a popular brand of high-current implanter is 13 6-inch wafers, 18 5-inch wafers, or 25 4-inch wafers. The ratios of these load sizes were used for converting 4-inch and 5-inch wafer operations per day into equivalent 6-inch wafer operations per day.

An important trend in integrated circuit design is the increasing number of metal layers. Most submicron logic process flows in our survey have two metal layers, and the most advanced

designs have three layers of metallization. Thus the productivity of metallization machines is of increasing interest. From our MOQ data it was possible for us to compute a throughput score for metallization machines. A variety of makes and models of metallization machines were observed in use at the participants, whereby different machines have different load sizes and processing times. Thus our throughput metric for metallization machines is once again a very aggregate metric. We define the *metallization machine throughput* metric as the average number of metal layers completed per machine per calendar day, considering the completed number of metal layers in the process flows of the fab in the numerator and considering only the number of metallization machines installed in the fab in the denominator. This metric is computed at the fab level by quarter going back several years. Similar to the case of ion implantation, some of our participants have multiple metallization operations in the same metal layer of a process flow; thus our metric for the number of metal layers completed is sometimes less than the number of metallization operations actually performed. Although the exact number of metal layers completed per day is not requested in our Mail-Out Questionnaire, we estimate this number MO for each process flow as

$$MWO = (WS/7)(NM)(LY'), \tag{7}$$

where WS is the average number of wafer starts per week for the process flow divided by 7 calendar days per week, NM the number of metal layers in the process flow, and LY' is the inflated line yield given by (5). (As before, this inflated line yield allows for half of the total line yield loss to load metallization, or equivalently, the average wafer that is scrapped makes it through exactly half of the metallization operations before being discarded.) Considering all process flows, the total metallization operations per day is computed, then divided by the number of metallization machines in service to obtain the value of the metric.

For fabs producing 4 inch or 5 inch wafers, conversion factors need to be applied to convert raw scores into 6-inch equivalent scores. Lacking any detailed information about machine processing times, we simply compared the wafer areas for 6-inch, 5-inch and 4-inch wafers. The ratios of the wafer areas were used to convert 4-inch and 5-inch wafer operations per day into equivalent 6-inch wafer operations per day.

Obtaining an overall fab efficiency metric is difficult. As a relatively simple step in this regard, we combined the stepper throughput metric with the integrated yield metric to obtain an *integrated stepper throughput* metric. This metric reduces stepper throughput by line yield and die yield losses to measure the equivalent number of perfect wafer layers processed per 5X stepper per day, assuming a product with die area of 0.5 sq cm was in production. For each process flow, the number of good wafer operations per day GWO is estimated as

$$GWO = (WS/7)(NS)(LY20)\left[\frac{1-e^{-(0.5)D}}{(0.5)D}\right]^2, \tag{8}$$

where WS is the average number of wafer starts per week for the process flow divided by 7 calendar days per week, NS the number of 5X stepper layers in the process flow, $LY20$ is the line yield metric calculated for the process flow using (1), and D is the defect density for the process flow

calculated using (2).

This integrated metric assists the reader in assessing the participants' effectiveness in addressing the intricate trade-offs between line yield, die yield and equipment throughput in their attempts to maximize overall good output.

2.3 Labor Productivity Metrics

Most fabs measure labor productivity in terms of the number of wafer "moves" per operator per day, where a move is credited each time one wafer completes a single processing step or some short sequence of steps. The granularity of what constitutes a "move" varies from fab to fab, and so we are forced to develop a more aggregate metric, as follows.

Wafer layers per operator per day is our direct labor productivity measure, simply measuring the average number of wafer layers completed per working day divided by the total number of operators employed by the fab. The number of wafer layers WL completed per working day for a particular process flow is estimated from the MOQ responses as

$$WL = (WS / WD) (NL) (LY'), \tag{9}$$

where WS is the average number of wafer starts per week for the flow, WD is the number of working days per week, NL is the total number of mask layers in the process flow, and LY' is the inflated line yield for the flow as defined by equation (5). The total number of wafer layers completed per working day is obtained by summing the figures for each process flow; the value of the metric is then obtained by dividing by the number of operators employed at the time. This metric was computed by quarter going back several years.

Operator productivity may be increased by reducing the manual work activity (e.g., automating material handling, automating machine recipe download, automating data logging, consolidating consecutive process steps into linked equipment clusters or into multi-chamber cluster tools), as well as by increasing the opportunity for operators to perform wafer operations (increasing equipment availability, decreasing machine processing time, staggering operator breaks, cross-training operators, etc.).

The definitions of who is included in direct labor and who is included in indirect labor varies among the participants, and there is a continuing trend at many fabs to blur the distinction between the two groups. *Wafer layers per total head count per day* is our total labor productivity measure, analogous to the direct labor productivity metric except that the denominator accounts for all fab employees, including dedicated staff from equipment vendors. This metric is of interest as it accounts for differences in the size of the engineering and administrative staffs of the fab participants.

2.4. The Cycle Time Metric

Cycle time per wafer layer, defined for each process flow, measures the average duration, expressed in fractional working days, consumed by production lots of wafers from time of release

into the fab until time of exit from the fab, divided by the number of mask layers (i.e., circuitry layers) in the process flow. This metric measures the average elapsed time to complete all operations associated with a single layer of circuitry, accounting for processing time, lot waiting time and lot movement time. This metric may be improved by reducing any one or all three of the foregoing components.

Reduction in fab cycle times can reflect the combined effects of many different kinds of improvements. Lot movement time can be reduced with fab layout changes and with automation of lot transfer and retrieval; lot waiting time can be reduced by improving equipment availability, by reducing the frequency and duration of out-of-control process holds, and by implementation of just-in-time control mechanisms and other efficient scheduling practices; and processing times can be reduced by the reduction or elimination of pre-process tests and setups, by automation of recipe download, by machine modifications that reduce machine jams and assists, etc.

The loading of the fab relative to its capacity can have a significant effect on cycle times. Fabs which transition from an underloaded status to a fully loaded status are likely to see an extension of their cycle times. Most but not all of the fabs in our sample were fully loaded throughout their four-year period of observation, as indicated in Tables 2.1 - 2.3.

Low cycle times are particularly important to manufacturers of custom integrated circuits (known as ASICs, an acronym standing for application-specific integrated circuits), for which sales from stocks of finished goods are not practicable. Cycle times are a concern even for producers of make-to-stock products, since shorter cycle times promote improved demand forecasting accuracy and thus better utilization of fab capacity and less inventory obsolescence. Some participants believe that low cycle times tend to be positively correlated with good values for other technical metrics such as yields and equipment efficiency; thus some companies use cycle time reduction efforts as a driver for general manufacturing improvements.

We computed the cycle time for each major process flow (up to a maximum of eight flows for each participating fab) by quarter going back several years, and then summarized the scores up to the fab level by computing a weighted average cycle time for the entire fab. The weights used were the number of wafer starts in each process flow.

2.5 Memory Fab Metric Scores

Figures 2.1 - 2.14 graph metric scores over time for the submicron memory fab participants. Numerical values of the most recent observation of each metric for each participant are presented in Tables 2.4 - 2.17. Memory fabs place a priority on maximizing integrated output, and thus are highly focussed on yield and equipment throughput. As will be discussed, they exhibit the highest throughput performance.

Line yield performance is depicted in Figure 2.1. Fabs M4, M6 and M10 achieve outstanding scores over many years, consistently maintaining line yields in the high 90s. Fab M3 achieved excellent scores very early (1989-1990), but then line yields declined at this fab as product mix was dramatically expanded to embrace a great variety of logic and memory devices. Fab M10 also exhibits a drop in line yields at the end of its time series, reflecting a substantial expansion of its product mix at that time. After a slow start, fab M9 catches up to the leaders in 1993, but it experiences a sharp drop at the end of its time series as well. After a poor startup in 1991-92, fab

M5 finally achieves very good scores in 1993-94. Fab M7 also had a poor start in 1991, but then achieves fair performance in 1992-93. Fabs M1 and M2 turned in fair to very good performances, while fab M8 seems far behind the leaders.

Figures 2.2 - 2.4 show defect density trends for the memory fabs, computed from die yields after laser repair. The vertical axes are base 10 logarithmic scales for the convenience of comparing rates of defect reduction. In these graphs and in defect density graphs for other fab categories discussed below, one curve is plotted for each process flow; sometimes, multiple curves for the same fab may appear in the same graph, reflecting the fact that data was received from the fab for more than one process flow belonging to the same category. Some curves have points for each quarter, while others have points for each month, depending on the level of detail of the data we received from the participants. In most cases, the initial point on each curve is data for the first month or quarter the process flow was qualified for production in the fab.

As can be seen, die yields are continually improved in nearly all process flows, albeit with occasional excursions reflecting parametric or particle problems that were difficult and/or expensive to solve. The downward slopes of the defect density curves reflect the prowess of the fab in deducing the sources of yield loss and rooting out such sources; a steeper slope is indicative of effective data collection and timely analysis concerning yield losses, and of ability to promptly realize technical and/or operational changes necessary to eliminate sources of yield loss.

Perhaps the most striking phenomenon observed here is that the starting points, i.e., the defect density scores in the first quarter of process life, have very great disparity. High starting defect densities can be caused by lack of conformance of product designs to process capabilities, lack of conformance of process specifications to equipment capabilities, or both. A high starting defect density is indicative that challenging product/process/equipment problems remain to be identified, characterized and solved by the manufacturing fab.

A review of the defect density graphs for both CMOS memory fabs and logic fabs (the latter to be discussed below) suggests that those fabs with poor starting points typically are not able to overtake those with good starting points, at least not for several years. Bearing in mind that most of the revenue potential of a semiconductor process flow is in the first several years of its life, the importance of a good initial defect density can not be underestimated. For example, a fab with a starting defect density that is six times worse than another but improves its defect density twice as fast still needs three years to catch up, by which time the revenue potential of the process flow may be mostly gone.

For one of its process flows in the 0.45 - 0.6 micron category, fab M6 achieves outstanding performance that is not matched until 1995 by fab M10. At that time, defects after repair have been driven down to about 0.2 per sq cm. In three other process flows operated by M6 in this category, the performance seems to match that of the other four participants. In the 0.7 - 0.9 micron category, fab M1 is the leader from 1992 onwards, driving defect density after repair down to 0.10 and less. Fab M1 achieves very good starting points in three of its flows in this category, but for one of its process flows, M1 experiences a very poor start. Despite the poor starting point, it is able to jump to leading-edge performance about 6 months later. This particular process technology was licensed from another semiconductor manufacturer; the graph suggests that perhaps some communication difficulties were encountered in the process transfer, but that the process flow itself was sound.

Fab M10's performance in the 0.7 - 0.9 memory category also is leading-edge in 1993. Fabs M3 and M4 were early entrants into this technology in 1990-91 and demonstrated leading-edge performance at the time. Incredibly, leading-edge performance in defect density in this category has improved from 1.00 to 0.10 defects per sq cm in only 3 years.

Figures 2.5 - 2.7 display the results of combining die yield and line yield performances in terms of the integrated yield metric. In the 0.45 - 0.6 micron category, the difference in performance evident in defect density scores is made more dramatic when integrated yield is displayed. Until 1995, one of the process flows operated by fab M6 stands far above the other process flows in this category. Note how almost every curve displays a "U" near the beginning, whereby yields initially decline as volume is ramped up and production problems are revealed. As these problems are solved over a period of months, the yield of each process flow climbs past its starting point. In the more mature 0.7 - 0.9 micron category, performance is more competitive, with fabs M3, M4, M6, M1 and M10 all defining the envelope of best performance at various points in time. In both the 0.45 - 0.6 and 0.7 - 0.9 micron categories of memory process flows, leading-edge integrated yields exceed 90 percent, a remarkable performance.

Figures 2.8 - 2.10 display equipment productivity trends for memory fabs. In Figure 2.8, 5X stepper throughput scores are graphed. In 1989-90, fabs M3 and M2 were early leaders, achieving about 450 wafer operations per stepper per day. In 1991, fab M4 overtakes them, reaching almost 600 wafer operations per machine per day. Fab M6 emerges as the leader in 1992, achieving almost 650 wafer operations per day in the second half of the year. Fabs M5 and M8 take over in late 1993 and 1994, also exceeding 600 wafer operations per stepper per day. Fab M10 achieves good throughput beginning in late 1994, while fabs M1 and M7 seem to be far behind the leaders.

Reviewing implanter productivity graphed in Figure 2.9, fab M3 was an early leader, achieving an outstanding 1400 implants per machine per day way back in 1989. Fab M6 emerges after 1993 to match this world-class performance. Fab M8 also shows good promise at the end of its time series in late 1993.

Metallization machine productivity is graphed in Figure 2.10. As before, fab M3 led the way in early years, achieving almost 150 wafer operations per machine per day. After 1992, fabs M5 and M8 take over, with surprisingly similar time series, reaching 250 wafer operations per machine per day by the end of 1993.

Figure 2.11 graphs our metric that integrates the yield and 5X stepper throughput metrics into a single score, plotting the equivalent number of full-wafer operations performed per stepper per day. This metric rises fairly steadily from 300 in 1989 to about 550 in 1992. Leadership shifts from fabs M2 and M3 to fab M4 and then to fab M6 over time. Fab M5 catches up to the leaders at the end of its time series in early 1994, as do fabs M4 and M10.

Cycle time for memory fabs is graphed in Figure 2.12. Fab M2 achieves good performance initially, but then cycle time increases at this fab in 1992. Fabs M6 and M7 both drive cycle time down to about 2.0 days per mask layer in 1993. Fab M5 operates at about 2.5 days per layer, while over half of the fabs in this category achieve cycle times of about 3 - 3.5 days per layer. Fab M10 is the laggard in this category, with an average cycle time exceeding 4 days per layer.

Turning to direct labor productivity, fabs M4, M6 and M10 all achieve a top score of about 70 wafer layers completed per operator per day, as shown in Figure 2.13. Considering the entire

fab headcount in Figure 2.14, fab M4 emerges as dominant, reflecting a remarkably low number of engineers reported in its MOQ. As this fab is sited adjacent to several other fab lines operated by the same company, it is possible some site-level staff that serve this fab were not recorded in our survey. On the other hand, productivity figures at fabs M6 and M10 approach and seem to confirm those of fab M4, pushing up towards 50 wafer layers completed per person per day.

The top labor productivity scores appearing in these figures (as well as in labor productivity figures for the other fab categories) reflect three key characteristics: (1) large size of the fab, whereby high-volume fabs with large banks of processing equipment need to employ the same or only slightly more operators and engineers than fabs with medium or small banks of equipment, (2) automation of lot and reticle (mask) movement, which decreases the amount of manual effort required in manufacturing, and (3) automation of recipe download, lot and equipment tracking, and equipment monitoring, which decreases the amount of manual information handling required in manufacturing. Apart from the effects of economies-of-scale, material handling automation, and information automation, labor productivity improves with increasing equipment efficiency, e.g., increasing equipment availability, eliminating or reducing pre-process tests and setups, etc.

2.6 CMOS Logic Fab Metric Scores

Figures 2.15 - 2.28 graph metric scores over time for the submicron CMOS logic fab participants. Numerical values of the most recent observation of each metric for each participant are presented in Tables 2.18 - 2.31. While high yield and high equipment throughput are also goals of CMOS logic fabs, many fabs in this category are also strongly focussed on cycle time control.

Line yield trends are depicted in Figure 2.15. Generally, scores are lower than for memory fabs, reflecting the challenge of producing a greater variety of devices in a smaller set of equipment. The most arresting feature of Figure 2.15 is the contrast between fabs with fairly steady, high line yields, and those who occasionally experience catastrophic events in which a considerable amount of work-in-process must be scrapped. Clearly, there are differences in the degree and effectiveness of process control among the participants.

Fabs L1, L5 and L16 turn in line yield scores in the high 90s, rivalling those of the focussed memory fabs. Fab L11 has a highly erratic time series. Part of this volatility is caused by its measurement scheme, in which lots on engineering hold are counted as yield loss, but then are "bonused" back in to production if released for continued processing by the engineer. This results in some of its scores at or exceeding 100 percent, while some of its other scores are extremely low.

Defect density trends for submicron CMOS logic fabs are graphed in Figures 2.16 - 2.18. In the 0.7 - 0.9 micron category, fab F8 displays an excellent performance, although this has to be viewed in light of a weak performance in line yield. Fabs L6, L11 and L1 also approach the leadership envelope after 1992. In the 1.0 - 1.25 micron category, the performance envelope is defined by fabs L9 and L4 in 1989-90, then fab L2 in 1991, and then fab L1 in 1992-93. Fab L5 reaches the envelope in 1994. A similar pattern is exhibited for the 1.3 - 1.5 micron category, with Fabs L11 and L6 initially defining the envelope, then fab L2, then fab L1, and then fabs L11 and L2 again. Over a period of 6 years, the leading-edge defect density was pushed down from 1.00 to about 0.20, about the same as for the 1.0 - 1.25 category. Best performance to date in the 0.7 - 0.9 category is 0.30 defects per sq cm, pushed down from 1.00 in only three years.

Figures 2.19 - 2.21 display integrated yields for these three CMOS logic categories. In the 0.7 - 0.9 category, it is remarkable how closely the time series for fabs L6 and L8 track, even though line yields and defect density scores were disparate. Perhaps the two fabs had different policies about scrapping lots in-line, but both policies led to the same integrated yield. ASIC fabs L11 and L1 achieve very high scores in 1992-93, while fabs L4 and L5 emerge with leadership scores in 1994. In the 1.0 - 1.25 micron category, the envelope is defined by fab L9 in 1989-92, with fab L2 catching up in 1991. Fabs L1, L5 and L16 catch up in 1993-94. In the 1.3 - 1.5 micron category, Fab L2 defines the envelope in 1990-92, with fabs L1 and L16 joining in from 1992 onwards. Leading-edge integrated yields reach about 80 percent in the 0.7 - 0.9 and the 1.0 - 1.25 categories, and reach about 85 percent in the 1.3 - 1.5 micron category.

Figures 2.22 - 2.24 depict equipment productivity scores for CMOS logic fabs. Throughput of 5X steppers is graphed in Figure 2.22. Generally, scores are lower than for memory fabs, perhaps reflecting the higher number of reticle changes that must be made as well as the concern for low cycle time. Fabs L9, L2 and L13 achieved leadership scores in 1989-90 of about 400 wafers per machine per day. In 1991 fab L8 joins the leaders, as does fab L5 in 1992 and fab L14 in 1993. The top score is about 600 6-inch wafer operations per stepper per day, achieved by fabs L5 and L14. This score exceeds the performance of many memory fabs with much more narrow product mixes.

Ion implanter productivity appears in Figure 2.23. Fab L9 turns in an initially outstanding performance of 1300-1400 wafer implants per machine per day during 1989 that is not matched. Its score subsequently declines to about 1200 as its product mix is broadened, which is matched by fabs L8 and L14 in 1992-93. Fabs L1 and L5 are also contenders, with scores exceeding 1000 implants per day.

Metallization machine productivity is graphed in Figure 2.24. Fab L8 turns in an amazing performance, exceeding 400 wafers processed per machine per day, but this should be viewed in light of the fact that this fab has only one process flow, and thus recipe changes of these machines are minimal. Fabs L5 and L14 are in second place with scores exceeding 250 wafers processed per machine per day.

Figure 2.25 graphs our integrated stepper metric, combining the 5X stepper throughput and yield metrics into an overall score. Fab L2 holds the lead until 1993, when fab L5 emerges as the star, with equivalent full-wafer operations per 5X stepper per day reaching 500. The performance of fab L8 is also notable, with integrated stepper throughput approaching 400 equivalent full-wafer operations.

Cycle time performance for CMOS logic fabs is depicted in Figure 2.26. The time series are quite noisy as the mix of process flows in each fab is varied over time. Fabs L11, L12, L3 and L16 all have brought cycle times down to about 2.0 days per mask layer. Fab L2 initially achieved such cycle times, but then its cycle times rose closer to 3.0 days per layer in 1992 as its product mix diversified.

Labor productivity trends for CMOS logic fabs are graphed in Figures 2.27 - 2.28. In Figure 2.27, the productivity of operators is led by fabs L2 and L9, both very large fabs producing both memory and logic products. Fabs L14 and L5 also seem to be pushing up towards the leading-edge score of 40 wafer layers processed per operator per day. Considering total

headcount as shown in Figure 2.28, once again the large fabs display the top scores. Fab L16 shows a very good second-place score, approaching 25 mask layers per person per day, with fabs L5 and L14 close behind.

2.7 MSI Fab Metric Scores

Figures 2.29 - 2.41 graph metric scores over time for the MSI fab participants. Numerical values of the most recent observation of each metric for each participant are presented in Tables 2.32 - 2.44. MSI fabs generally utilize older generations of processing equipment for which process control is more difficult. These fabs produce a relatively large number of die types in a variety of Bipolar, BiCMOS and CMOS process flows, making yield analysis quite challenging.

Line yields for MSI fabs are depicted in Figure 2.29. In general, line yields are less consistent and lower than for the advanced CMOS fabs, perhaps reflecting the older age of the MSI fabs. These fabs feature more manual wafer and lot handling the the advanced CMOS fabs, and computerized recipe download and on-line monitoring is more difficult or sometimes impossible. Only fabs B6 and B2 report line yields per twenty layers exceeding 90 percent. Fabs B1, B7 and B8 exhibit serious deteriorating trends. Fab B3 experiences a major drop in line yields in the third quarter of 1992 from otherwise middle-of-the-road performance, while fab B5 improves to fair performance after a very poor start.

Most of the MSI fabs manufacture products in Bipolar process flows. Products produced in such process flows are characterized by parametric yield losses that rival or exceed defect-generated losses. Thus defect density scores for the MSI fabs are far less meaningful than for the advanced CMOS fabs. Several of our MSI participants manufacture very small die in Bipolar process flows, and even though their calculated defect densities are high, their die yields are not very low.

Keeping this concern in mind, defect density scores for three process technology categories may be viewed in Figures 2.30 - 2.32. In the 1.2 - 3.5 micron Bipolar category, fab B6 achieves excellent scores, driving its scores down to the 0.50 - 0.20 range. In the 5 - 10 micron Bipolar category, fab B1 achieves the lowest score of 0.5 defects per sq cm for one of its process flows. Its performance in two other process flows in this category are more comparable to that of the flows in fabs B8 and B3. In the 1.5 - 4.0 micron CMOS and BiCMOS category, fab B5 is the leader, followed closely by fabs B1 and B2. Best scores in this category are about 1.0 defects per sq cm.

Figures 2.33 - 2.35 display the results from combining line yield and defect density scores into an integrated yield metric. A die size of 0.5 sq cm is assumed to estimate die yields using the Murphy defect density formula (2). Based on its top performance in both line yield and die yield categories, fab B6 is the clear top performer in the 1.2 - 3.0 micron Bipolar category, with an excellent integrated yield score of 90 percent. Fab B6 is also the top performer in the 3.5 - 10.0 micron Bipolar category, with an integrated yield exceeding 80 percent. In the 1.5 - 4.0 micron CMOS category, scores are generally weak, with fabs B5 and B2 exhibiting the top scores, only in the low 50s.

Equipment productivity trends for MSI fabs are shown in Figures 2.36 - 2.38. Only two of our MSI fab participants were using 5X steppers at the time of our survey. Their scores are

depicted in Figure 2.36. Fab B3 exhibits an excellent performance, achieving nearly 800 wafer operations per stepper per day at the end of its time series, the best performance of any fab in any category, and an outstanding achievement. Fab B2 achieves good scores in 1990-91, but then performance drops as the volume fell off sharply in this fab. At the end of its time series, volume was beginning to recover in fab B2, and scores are likely much higher in more recent times.

Ion implanter productivity is depicted in Figure 2.37. Only fab B3 shows a good performance, achieving almost 800 wafer implants per machine per day in the second half of 1993. Figure 2.38 displays metallization machine productivity. Once again fab B3 shows good performance, achieving 200 wafer operations per machine per day. Fab B2 also achieved such throughput in 1989, but performance fell off sharply in subsequent years as volume in this facility was curtailed.

Cycle time performance of MSI fabs is graphed in Figure 2.39. Fab B3 is clearly the leader in this regard, registering an outstanding score of about 1.2 days per mask layer and maintaining performance in the range of 1.2 - 1.5 days per layer over the two years until the end of its time series. Fab B3's scores are even more remarkable in light of the fact that, at the same time, this fab also registered the highest equipment productivity among MSI fabs. Fab B7 exhibited excellent cycle times until mid-1993, but then cycle times increased dramatically after that as volume was ramped up and the number of process flows under development was increased in this fab.

Labor productivity trends for MSI fabs are displayed in Figures 2.40 - 2.41. As shown in Figure 2.40, fabs B1 and B3 exhibit top scores in operator productivity, processing about 55 wafer layers per operator per day. These two fabs also achieve the highest scores among MSI fabs in total labor productivity, processing about 30 wafer layers per headcount per day, as depicted in Figure 2.41.

2.7 Special Factors Underlying the Metric Scores

In Chapter 3, we investigate aspects of fab performance more closely, and we correlate managerial, technical and organizational practices with the foregoing metric scores. This analysis serves to identify those practices characteristic of top manufacturing performance. But beforehand, it is worth identifying several salient factors concerning fab size and configuration, fab operating schedules, and product design rules that strongly underlie the metric scores.

The first factor is fab size. Small fabs suffer from what some fab managers call a "granularity effect". As discussed above, small fabs inevitably do not achieve high labor productivity scores. This effect applies to equipment productivity as well. To illustrate, consider Figure 2.21. Fab L10 exhibits a very low 5X stepper throughput score. This fab has only one process flow requiring the use of 5X steppers, and its use is only required on a couple of critical mask layers. All other layers may be exposed using projection aligners. The production workload requires about 0.3 5X steppers, so the fab must have at least one stepper in service. But if this stepper is down for a significant length of time, the entire process flow is blocked, and cycle times may prove to be unacceptable. So the fab has two such machines in use, making for poor stepper productivity. On the other hand, a larger fab whose designed production load calls for, say, 12 machines, sees a much smaller percentage of excess capacity if, say, 14 machines are installed to mitigate cycle times. Hence both equipment and labor productivity numbers generally are inferior for small fabs.

The second factor is fab operating schedule. Because of labor agreements or other factors, some fabs do not operate fully-manned shifts 24 hours 7 days a week, and/or they may have more frequent holiday shut-downs than other fabs. Such limited operating schedules have strong negative effects on the cycle time and equipment productivity metrics. Given that quite a number of fabs are fully staffed around the clock almost every day of the year, a fab not fully staffed every day is unlikely to achieve leading scores in these metrics, no matter how proficient is its management and technical staff.

The third factor is product design rules. Given two manufacturers operating the same process flow using the same equipment set, one would expect the die yields at the manufacturer with more restrictive design rules (that is, more restrictive on the design of the product, but more generous in terms of manufacturability) should be higher than at the manufacturer with less restrictive design rules, at least in the early life of the process when there are likely to be significant parametric problems. While we have no quantitative measures of design rules enforced by the participants of the CSM study, we have been led to believe that ASIC manufacturers generally have more restrictive design rules than do makers of standard logic products. Indeed, ASIC manufacturers account for two out of the top three positions in the 0.7-0.9 micron CMOS logic category for the defect density metric.

The fourth factor is the use of SMIF (standard mechanical interface) technology. SMIF involves the application of plexiglass housings around each processing machine and around each production lot. In addition, there is special air handling arranged within and above each machine housing, as opposed to uniform air handling throughout the clean room, as is customary. SMIF thereby affords a cleaner environment for lots and machines than for the rest of the clean room. Standard mechanical interfaces allow operators to simply tender the clean boxes containing lots to an end station on the clean housing of a processing machine, whereby mechanical equipment takes care of all transfer of wafers between lot box and processing machine. Two of our participants have fabs featuring SMIF technology applied throughout the fab (with the exception of sputter and diffusion areas, where SMIF is difficult to apply), and one other participant has SMIF enclosures surrounding only its steppers handling critical layers.

SMIF is a "die yield enabler" in the sense that it can help achieve cleanliness standards beyond the designed capability of the clean room. It enables older and/or more modest clean rooms to operate advanced process flows with die yields that are competitive with newer and more expensive clean rooms. It is thus effective at extending the life of clean rooms; in fact, by virtue of SMIF, one of our participants achieved leading-edge defect densities in a relatively old and relatively modest clean room. To achieve excellent die yields, the management of a fab equipped with SMIF still needs to develop strong data collection and analysis capabilities as well as a strong problem-solving organization able to quickly identify and solve yield problems, but nonetheless SMIF technology can endow older fabs with the potential to be successful operating advanced process flows.

Another aspect of SMIF is that the technology may be installed supplemented by substantial error-prevention and information handling automation. These features tend to increase line yields, reduce cycle times, and increase labor productivity by virtue of mistake-proofing manufacturing and eliminating manual information handling.

The last factor concerns the age of the processing equipment. Generally, newer generations of processing equipment perform processing operations with more parametric precision and with deposition of fewer undesired particles than can be achieved by older generations of equipment. Typically, processing equipment can be utilized over three or four generations of process flows with ever-shrinking geometries. The most critical or difficult steps in a new-generation process flow may require the latest or next-to-latest generation of processing equipment.

This factor is important because there is significant variation among our participants in the equipment sets utilized to operate comparable process flows. As the most extreme example, one of our participants in both the memory and CMOS logic categories operates submicron process flows in a fab that consists entirely of used processing equipment. As might be expected, this fab scores higher defect densities than most of our other participants. As another example, another participating fab prides itself on "getting high mileage" out of its processing equipment using mix-and-match strategies to apply new processing equipment to process flows only at critical steps where such application is essential, while using older equipment at all other steps. Equipment bays in this fab are humorously described by the fab management as "museums", in that many or even all generations of the processing equipment are present. This fab's defect density scores are middle-of-the-road compared to our other participants. While these two fabs are not leaders in the defect density metrics, it may well be that their die *cost* is very competitive or even in leadership position, considering the reduced capital cost of their fabrication plant.

Ideally, we should devise a metric that measures the total amount of good circuitry or good silicon produced per capital dollar invested, in order to sort out the trade-off between lower-cost equipment and the higher die yields enabled by newer and more expensive processing equipment. This metric would have to examine output and machine stocks over a long period of time, and so it is not easy to implement. We hope to develop such a metric in the future.

With these performance factors as a background, we now turn to managerial, technical and organizational practices that also serve to explain differences in performance.

Figure 2.1. Memory Fab Line Yield

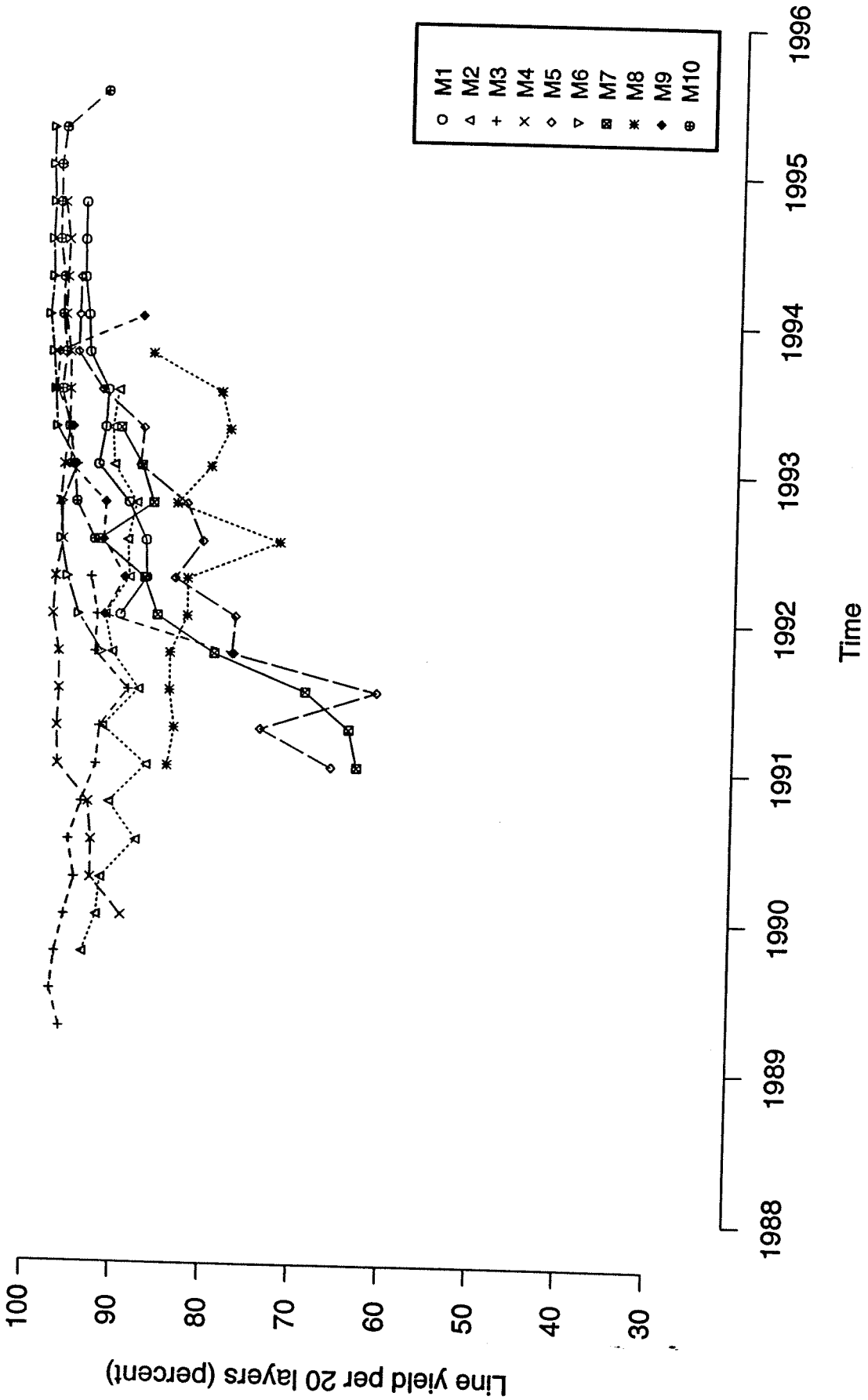
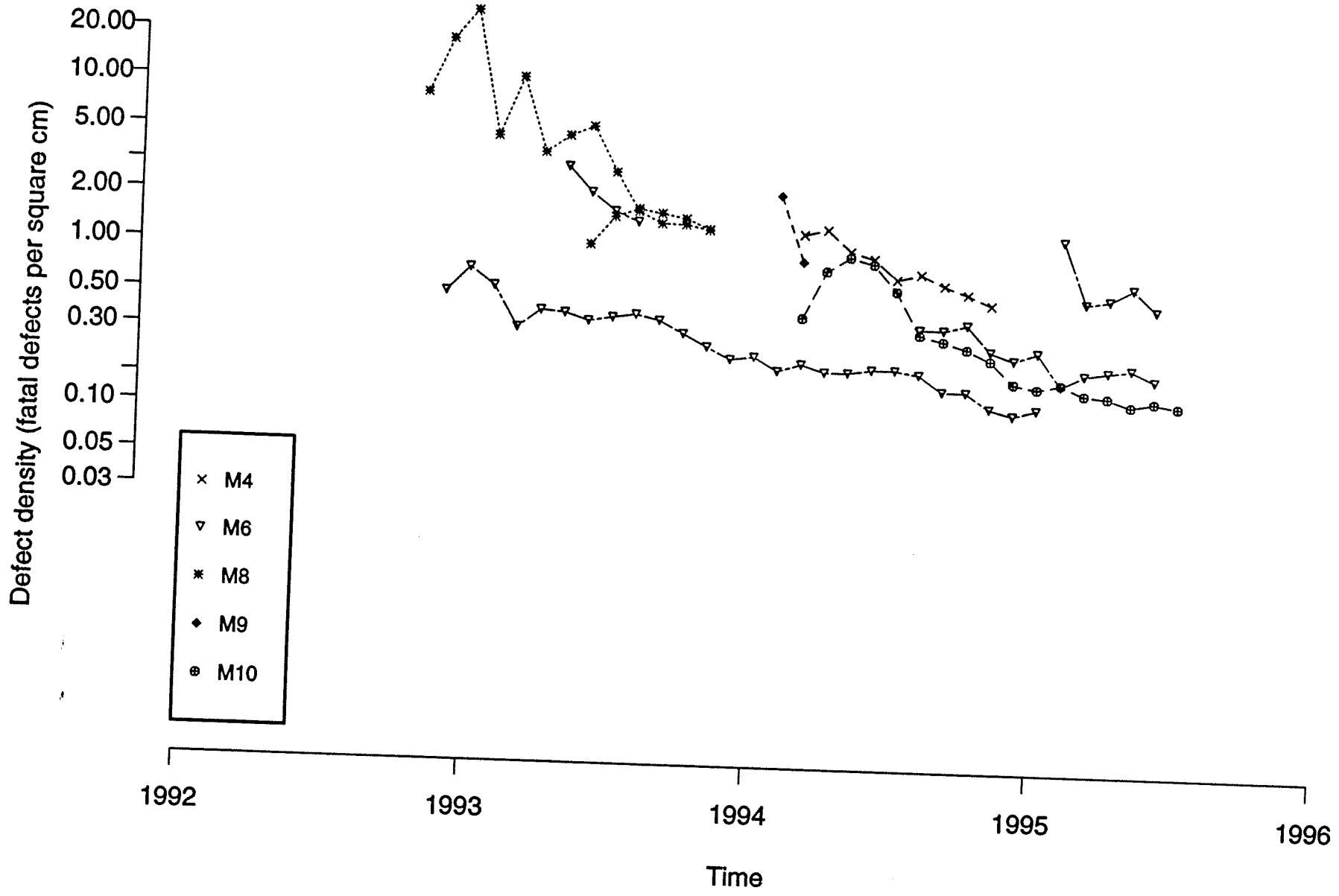


Figure 2.2. Memory Fab Defect Density

0.45 - 0.6 micron CMOS process flows



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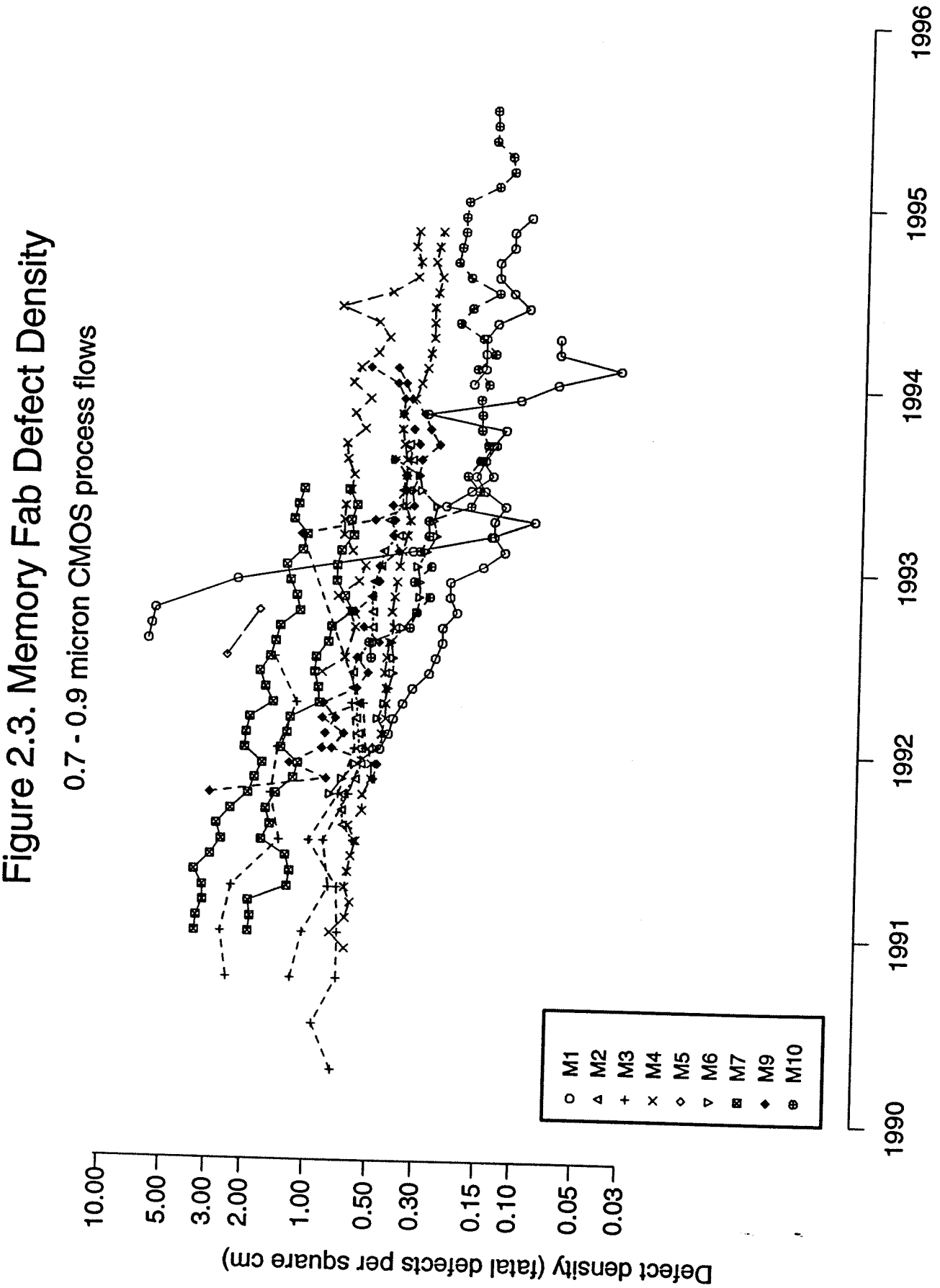


Figure 2.3. Memory Fab Defect Density
0.7 - 0.9 micron CMOS process flows
Defect density (fatal defects per square cm)
10.00
5.00
3.00
2.00
1.00
0.50
0.30
0.15
0.10
0.05
0.03
1990
1991
1992
1993
1994
1995
1996
Time
M1
M2
M3
M4
M5
M6
M7
M9
M10

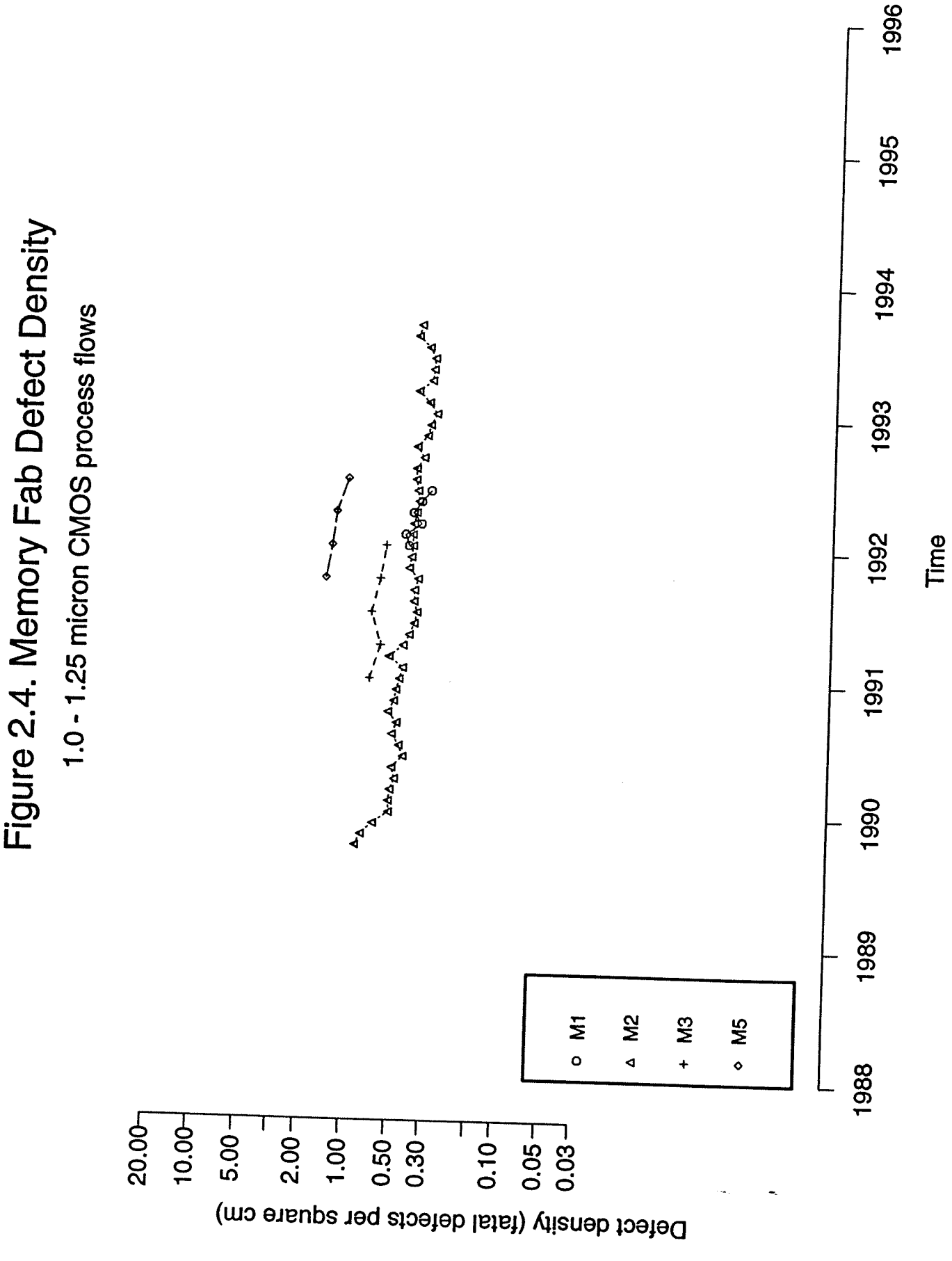


Figure 2.4. Memory Fab Defect Density
1.0 - 1.25 micron CMOS process flows
Defect density (fatal defects per square cm)
20.00
10.00
5.00
2.00
1.00
0.50
0.30
0.10
0.05
0.03
M1
M2
M3
M5
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time

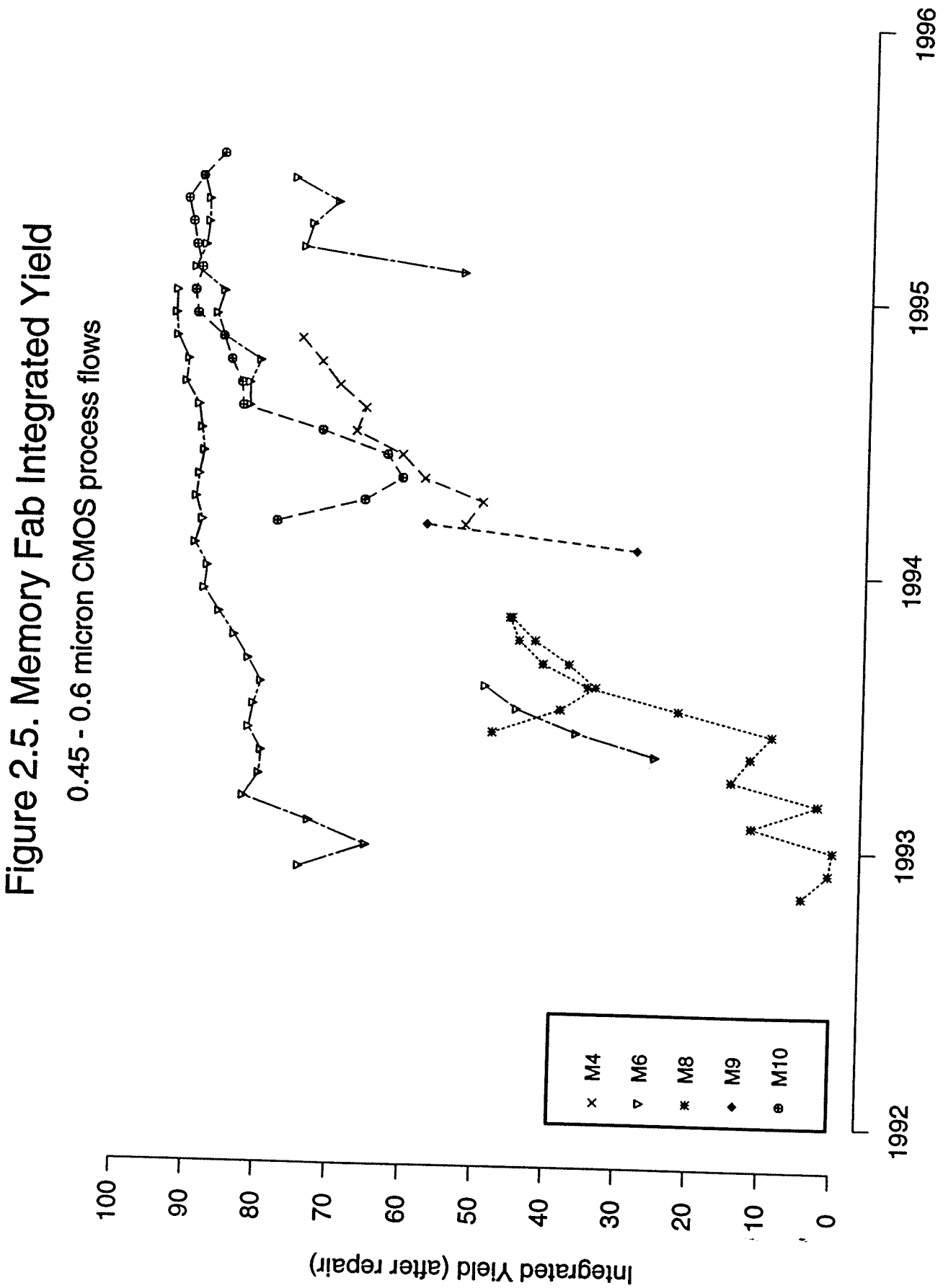


Figure 2.5. Memory Fab Integrated Yield
0.45 - 0.6 micron CMOS process flows
Integrated Yield (after repair)
100
90
80
70
60
50
40
30
20
10
0
1992
1993
1994
1995
1996
Time
M4
M6
M8
M9
M10

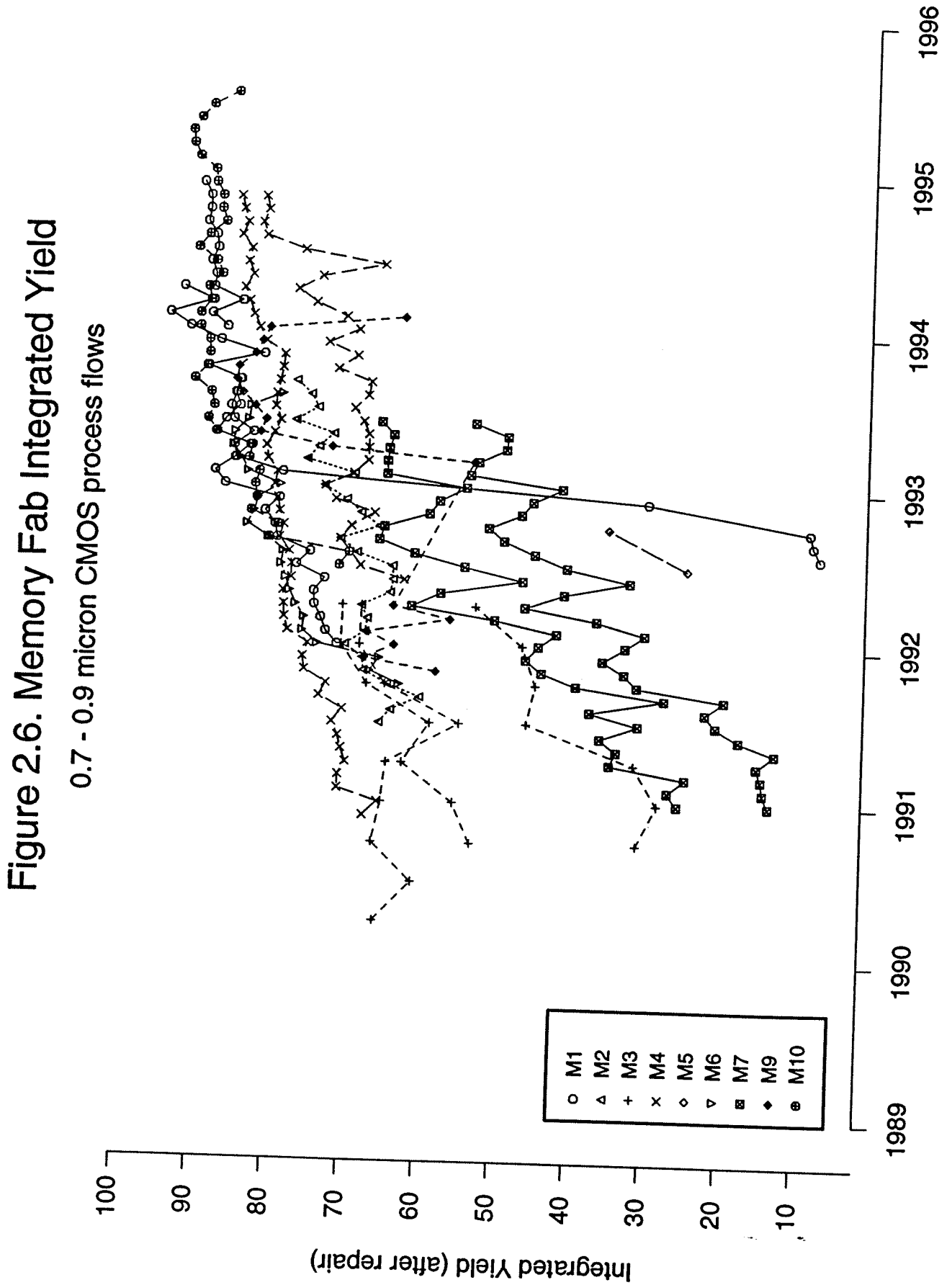


Figure 2.6. Memory Fab Integrated Yield
0.7 - 0.9 micron CMOS process flows
Integrated Yield (after repair)
100
90
80
70
60
50
40
30
20
10
1989
1990
1991
1992
1993
1994
1995
1996
Time
M1
M2
M3
M4
M5
M6
M7
M9
M10

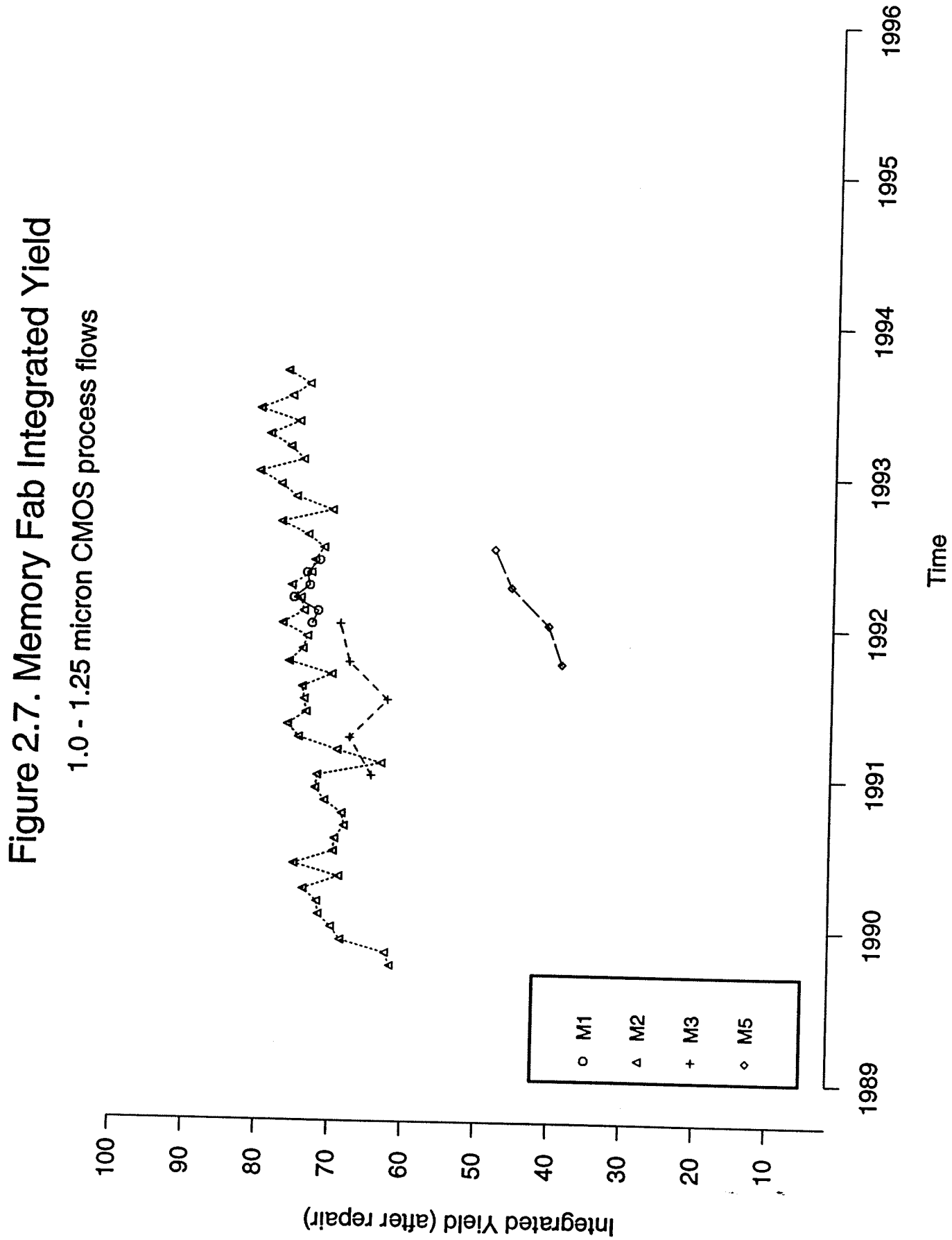


Figure 2.7. Memory Fab Integrated Yield

1.0 - 1.25 micron CMOS process flows

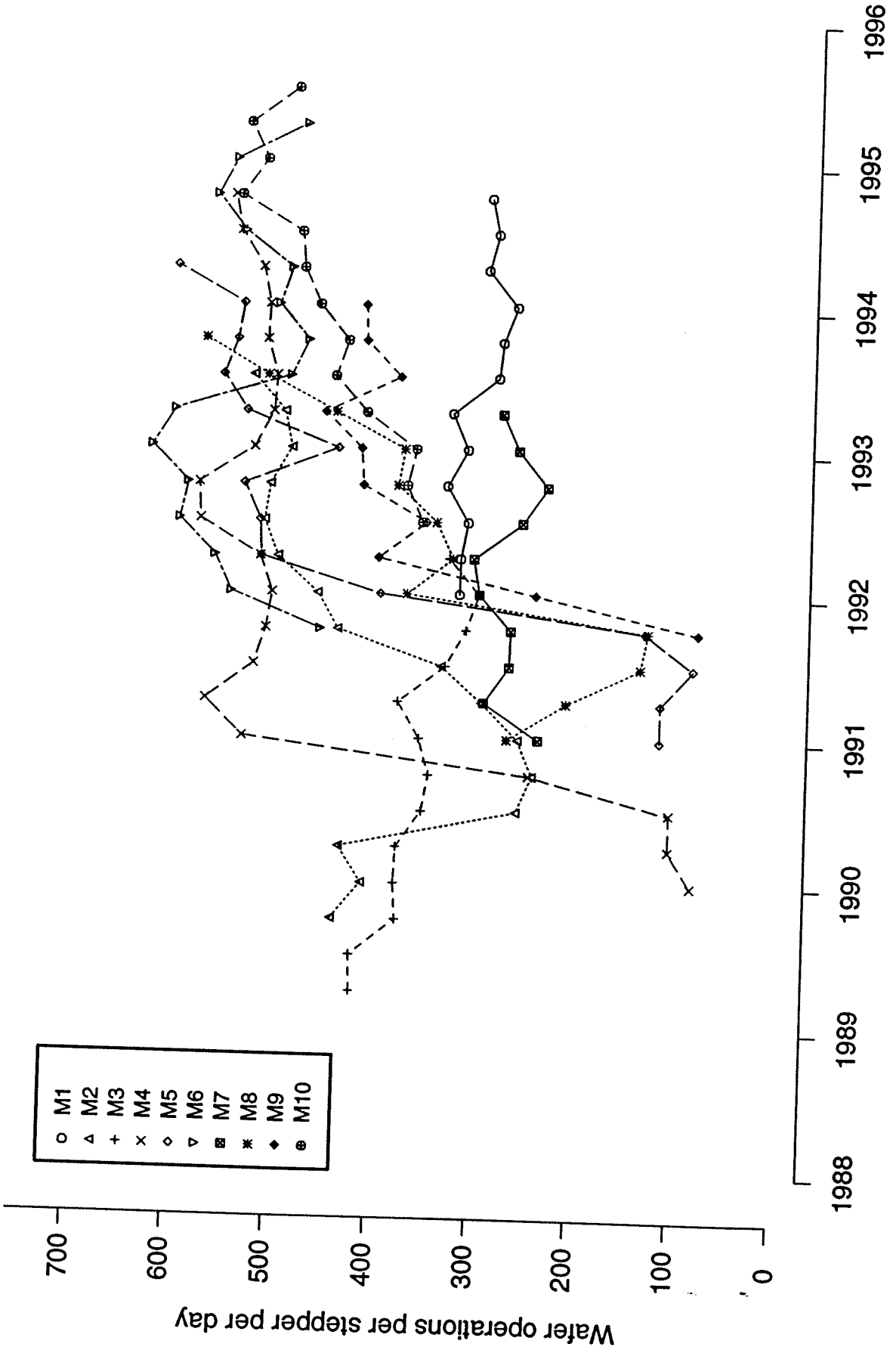


Figure 2.8. Memory Fab 5X Stepper Productivity

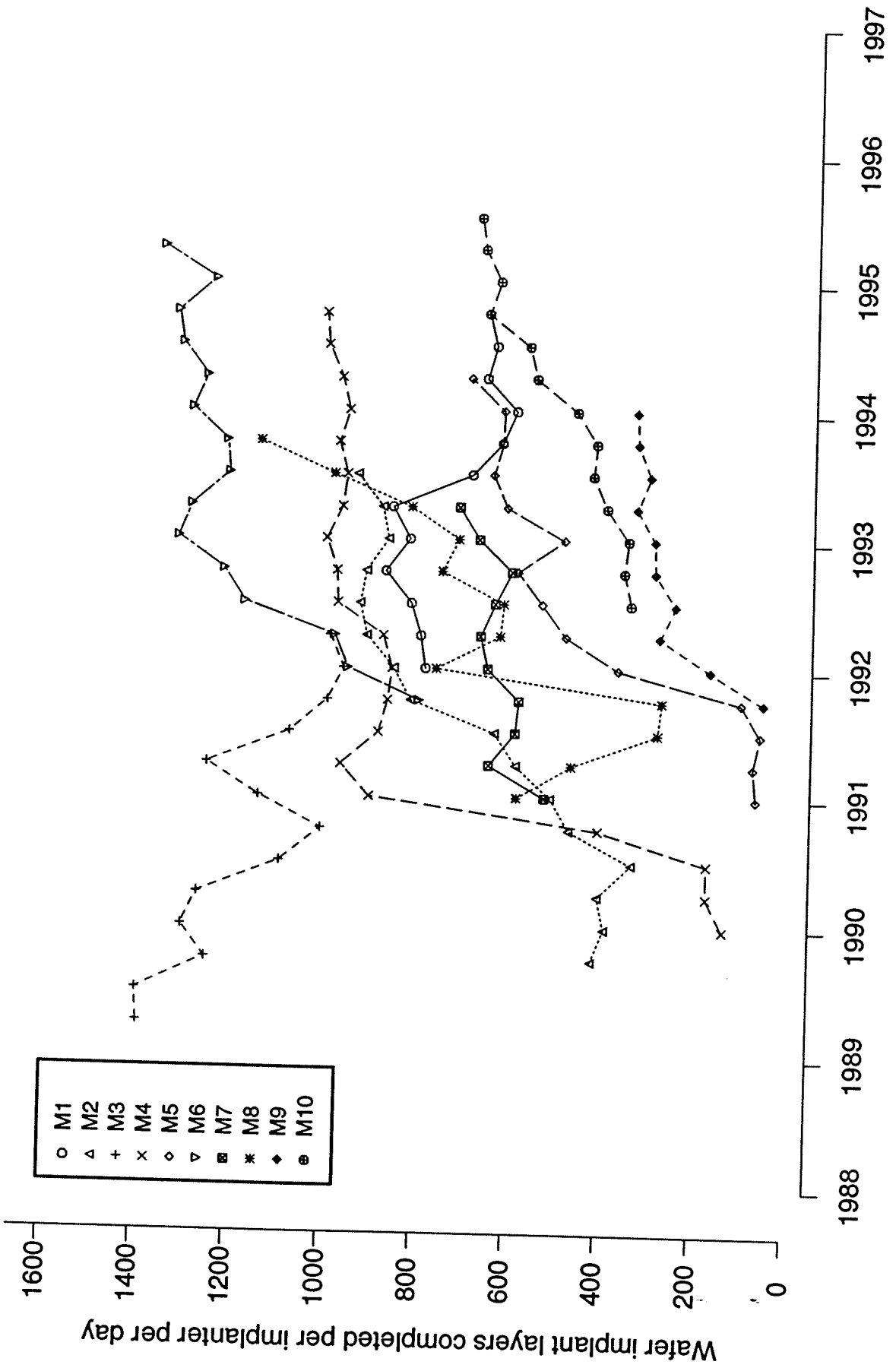


Figure 2.9. Memory Fab Ion Implanter Productivity

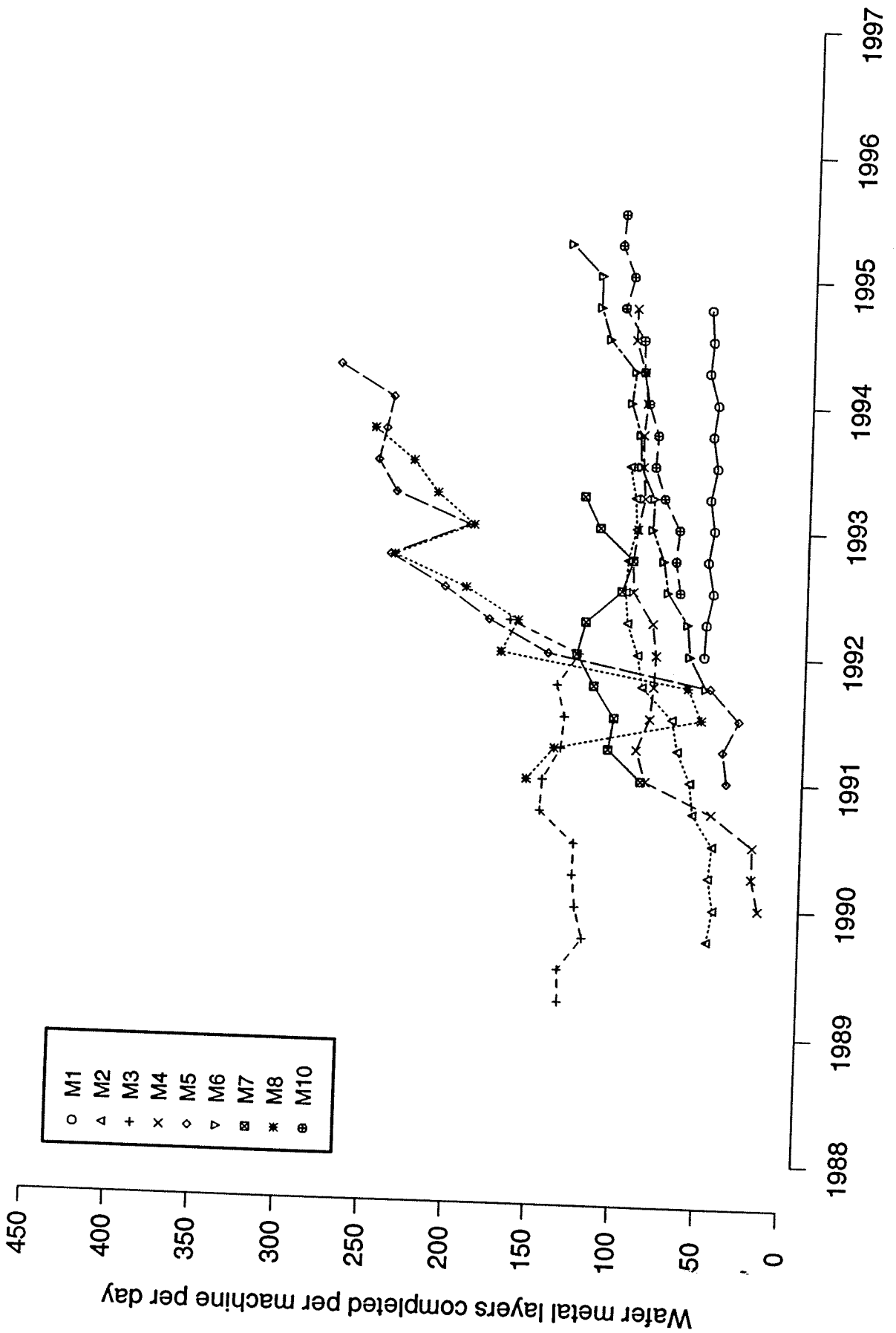


Figure 2.10. Memory Fab Metallization Machine Productivity
Wafer metal layers completed per machine per day
0
50
100
150
200
250
300
350
400
450
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
Time
M1
M2
M3
M4
M5
M6
M7
M8
M10

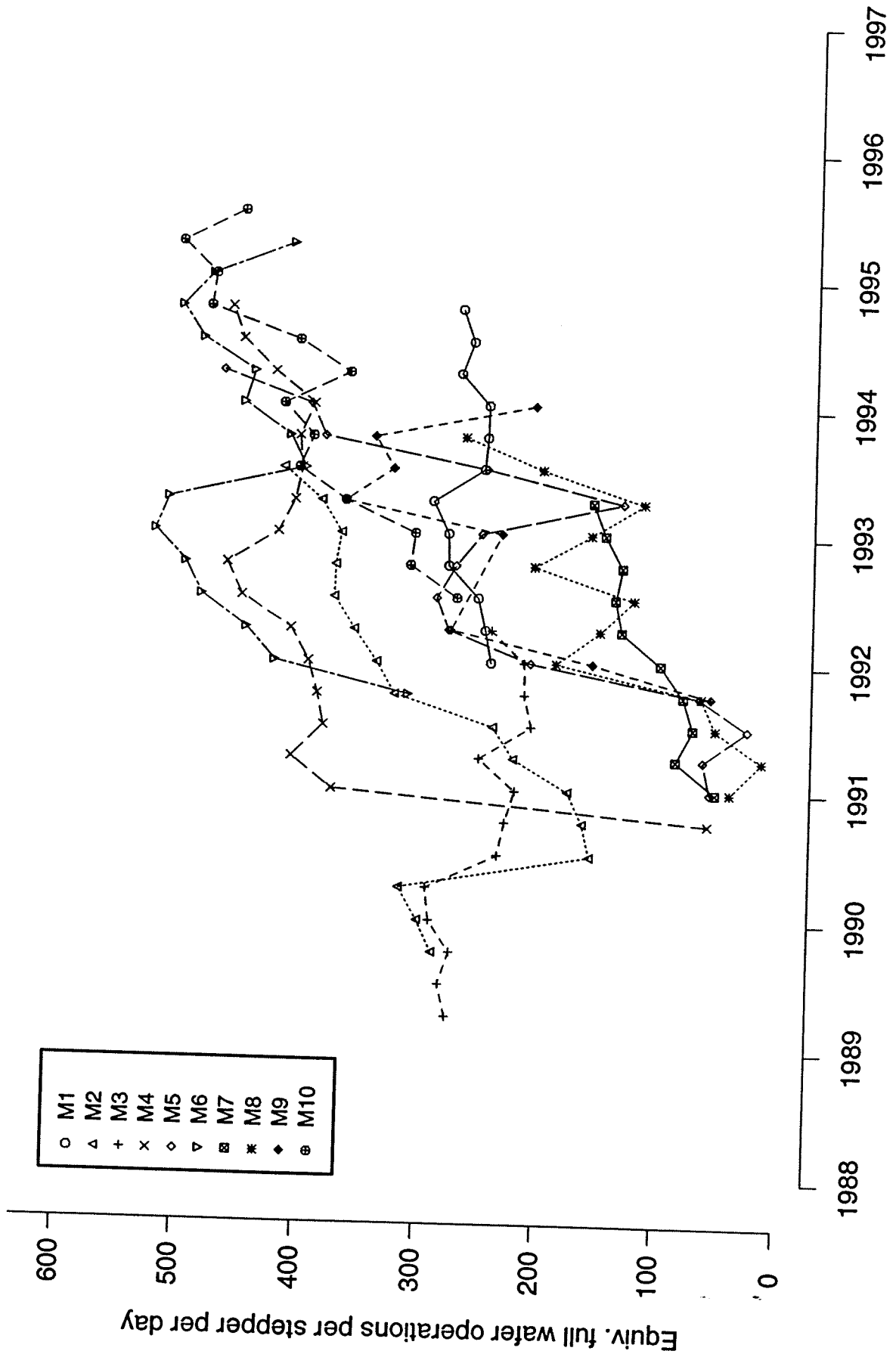


Figure 2.11. Memory Fab Integrated 5X Stepper Throughput
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
600
500
400
300
200
100
0
Equiv. full wafer operations per stepper per day
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
Time

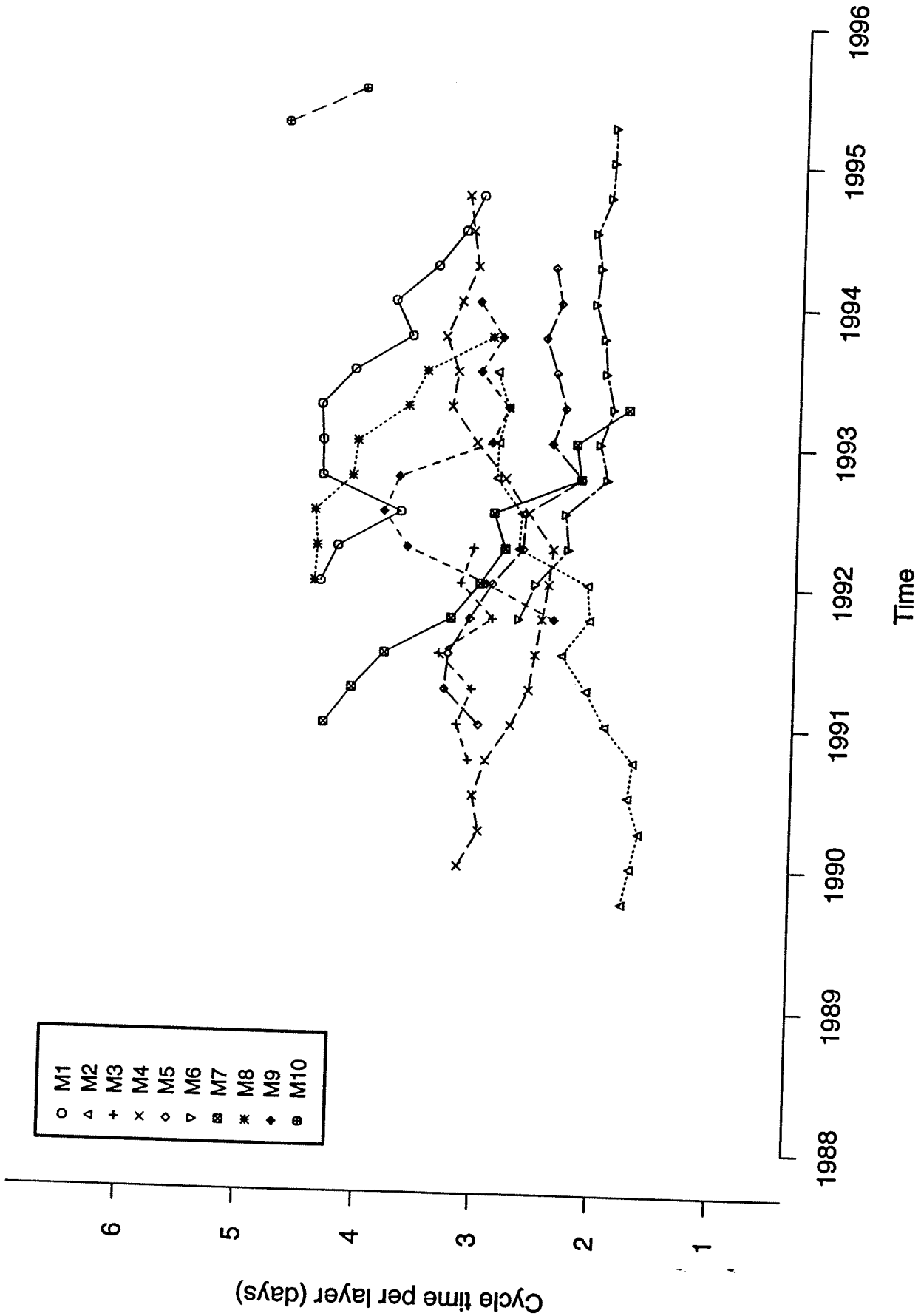


Figure 2.12. Memory Fab Cycle Time Per Layer
Cycle time per layer (days)
1
2
3
4
5
6
Time
1988
1989
1990
1991
1992
1993
1994
1995
1996
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10

Figure 2.13. Memory Fab Direct Labor Productivity

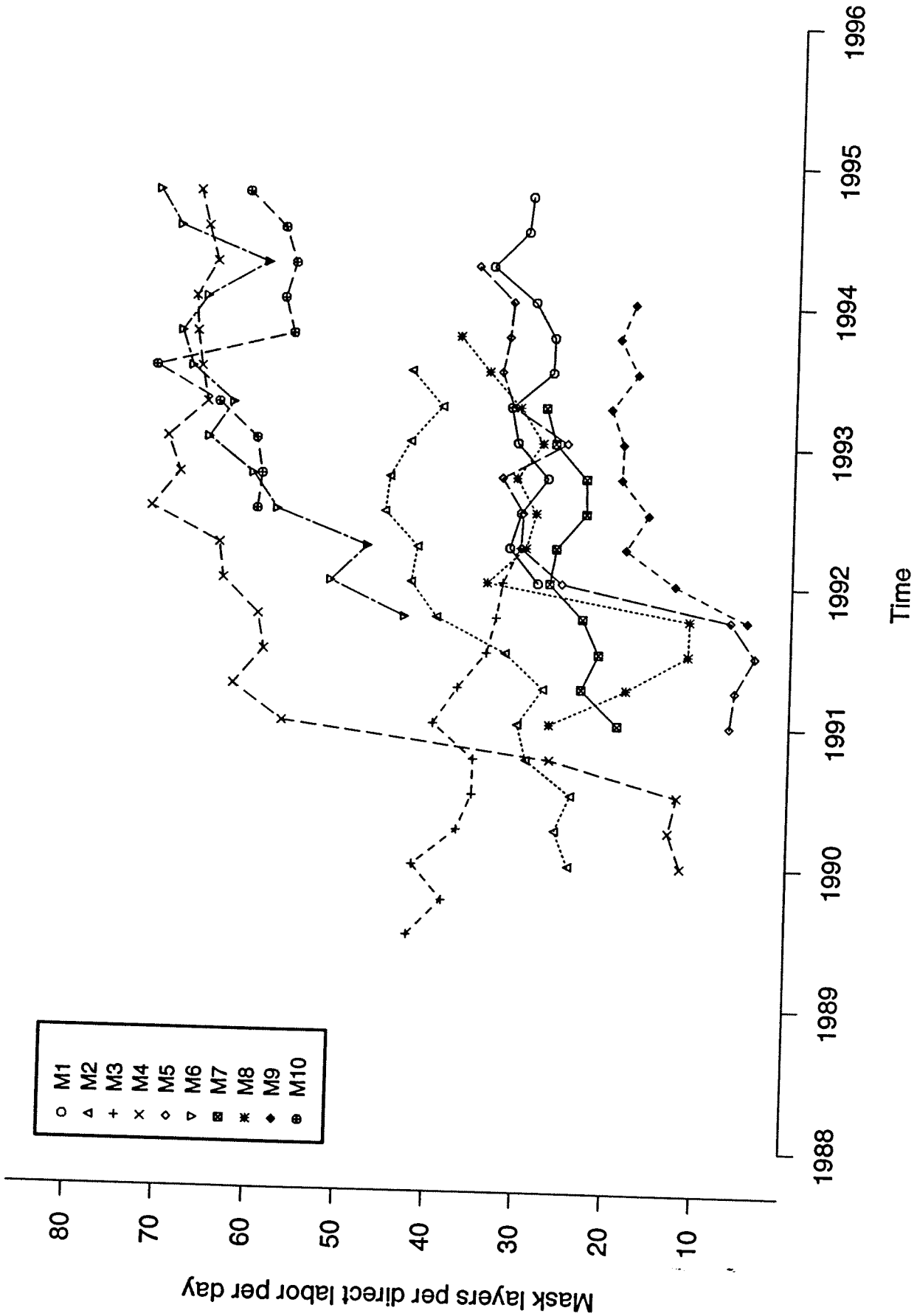


Figure 2.14. Memory Fab Total Labor Productivity

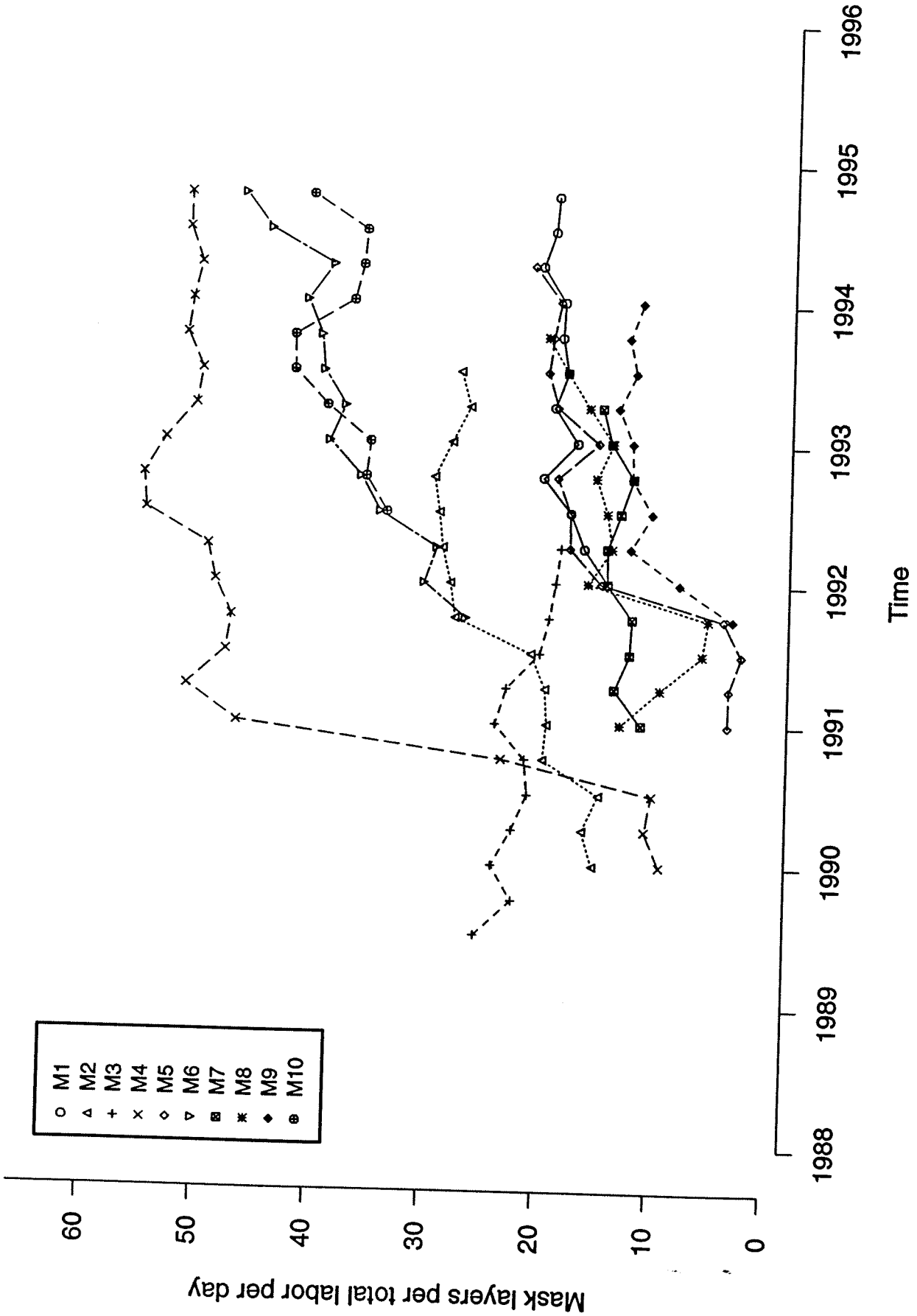


Table 2.4
Memory Fab Line Yields

Fab ID	Time	Line yield per 20 mask layers
M1	4Q94	95.0
M2	3Q93	90.9
M3	2Q92	93.5
M4	4Q94	97.4
M5	2Q94	95.4
M6	**2Q95**	**98.8**
M7	2Q93	90.5
M8	4Q93	87.1
M9	1Q94	88.3
M10	3Q95	92.8

Table 2.5
Memory Fab Defect Densities
0.45 - 0.6 micron CMOS process flows

Fab ID	Time	Murphy defect density after repair
M4	4Q94	0.52
M6	2Q95	0.19
M8	4Q93	1.34
M9	1Q94	0.89
M10	**3Q95**	**0.03**

Table 2.6
Memory Fab Defect Densities
0.7 - 0.9 micron CMOS process flows

Fab ID	Time	Murphy defect density after repair
M1	2Q94	0.07
M2	3Q93	0.36
M3	2Q92	0.57
M4	4Q94	0.26
M5	4Q92	1.81
M6	3Q93	0.42
M7	2Q93	0.69
M9	1Q94	0.42
M10	**3Q95**	**0.01**

Table 2.7
Memory Fab Defect Densities
1.0 - 1.25 micron CMOS process flows

Fab ID	Time	Murphy defect density after repair
M1	**2Q92**	**0.31**
M2	3Q93	0.38
M3	1Q92	0.60
M5	3Q92	1.08

Table 2.8
Memory Fab Integrated Yields
0.45 - 0.6 micron CMOS process flows

Fab ID	Time	Integrated line and die yield after repair (0.5 sq cm die)
M4	4Q94	75.5
M6	2Q95	89.7
M8	4Q93	46.0
M9	1Q94	57.8
M10	**3Q95**	**91.7**

Table 2.9
Memory Fab Integrated Yields
0.7 - 0.9 micron CMOS process flows

Fab ID	Time	Integrated line and die yield after repair (0.5 sq cm die)
M1	**2Q94**	**92.9**
M2	3Q93	77.8
M3	2Q92	70.9
M4	4Q94	85.6
M5	4Q92	35.9
M6	3Q93	79.5
M7	2Q93	66.3
M9	1Q94	63.7
M10	3Q95	92.7

Table 2.10
Memory Fab Integrated Yields
1.0 - 1.25 micron CMOS process flows

Fab ID	Time	Integrated line and die yield after repair (0.5 sq cm die)
M1	2Q92	72.3
M2	**3Q93**	**77.0**
M3	1Q92	69.3
M5	3Q92	48.3

Table 2.11
Memory Fab 5X Stepper Throughput

Fab ID	Time	Wafer operations per 5X stepper per day
M1	4Q94	297
M2	3Q93	528
M3	2Q92	331
M4	4Q94	551
M5	**2Q94**	**606**
M6	1Q95	549
M7	2Q93	281
M8	4Q93	575
M9	1Q94	419
M10	3Q95	490

Table 2.12
Memory Fab Ion Implanter Throughput

Fab ID	Time	Wafer operations per implanter per day
M1	4Q94	661
M2	3Q93	940
M3	2Q92	992
M4	4Q94	1010
M5	2Q94	698
M6	**2Q95**	**1360**
M7	2Q93	718
M8	4Q93	1146
M9	1Q94	339
M10	3Q95	682

Table 2.13
Memory Fab Metallization Machine Throughput

Fab ID	Time	Wafer operations per machine per day
M1	4Q94	53
M2	3Q93	99
M3	2Q92	169
M4	4Q94	97
M5	**2Q94**	**273**
M6	2Q95	137
M7	2Q93	136
M8	4Q93	252
M10	3Q95	106

Table 2.14
Memory Fab Integrated 5X Stepper Throughput

Fab ID	Time	Equiv. full wafer operations per machine per day
M1	4Q94	273
M2	3Q93	419
M3	2Q92	244
M4	4Q94	463
M5	2Q94	469
M6	**1Q95**	**479**
M7	2Q93	160
M8	4Q93	269
M9	1Q94	210
M10	3Q95	454

Table 2.15
Memory Fab Cycle Time

Fab ID	Time	Cycle time per mask layer (days)
M1	4Q94	3.1
M2	3Q93	2.9
M3	2Q92	3.1
M4	4Q94	3.2
M5	2Q94	2.4
M6	2Q95	2.0
M7	**2Q93**	**1.8**
M8	4Q93	2.9
M9	1Q94	3.1
M10	3Q95	4.1

Table 2.16
Memory Fab Direct Labor Productivity

Fab ID	Time	Wafer mask layers completed per operator per day
M1	4Q94	30.2
M2	3Q93	43.4
M3	2Q92	30.8
M4	4Q94	67.2
M5	2Q94	36.1
M6	**4Q94**	**71.7**
M7	2Q93	28.1
M8	4Q93	38.0
M9	1Q94	18.4
M10	4Q94	61.8

Table 2.17
Memory Fab Total Labor Productivity

Fab ID	Time	Wafer mask layers completed per person per day
M1	4Q94	19.4
M2	3Q93	27.6
M3	2Q92	18.5
M4	**4Q94**	**51.6**
M5	2Q94	21.3
M6	4Q94	46.8
M7	2Q93	15.1
M8	4Q93	20.0
M9	1Q94	11.8
M10	4Q94	40.9

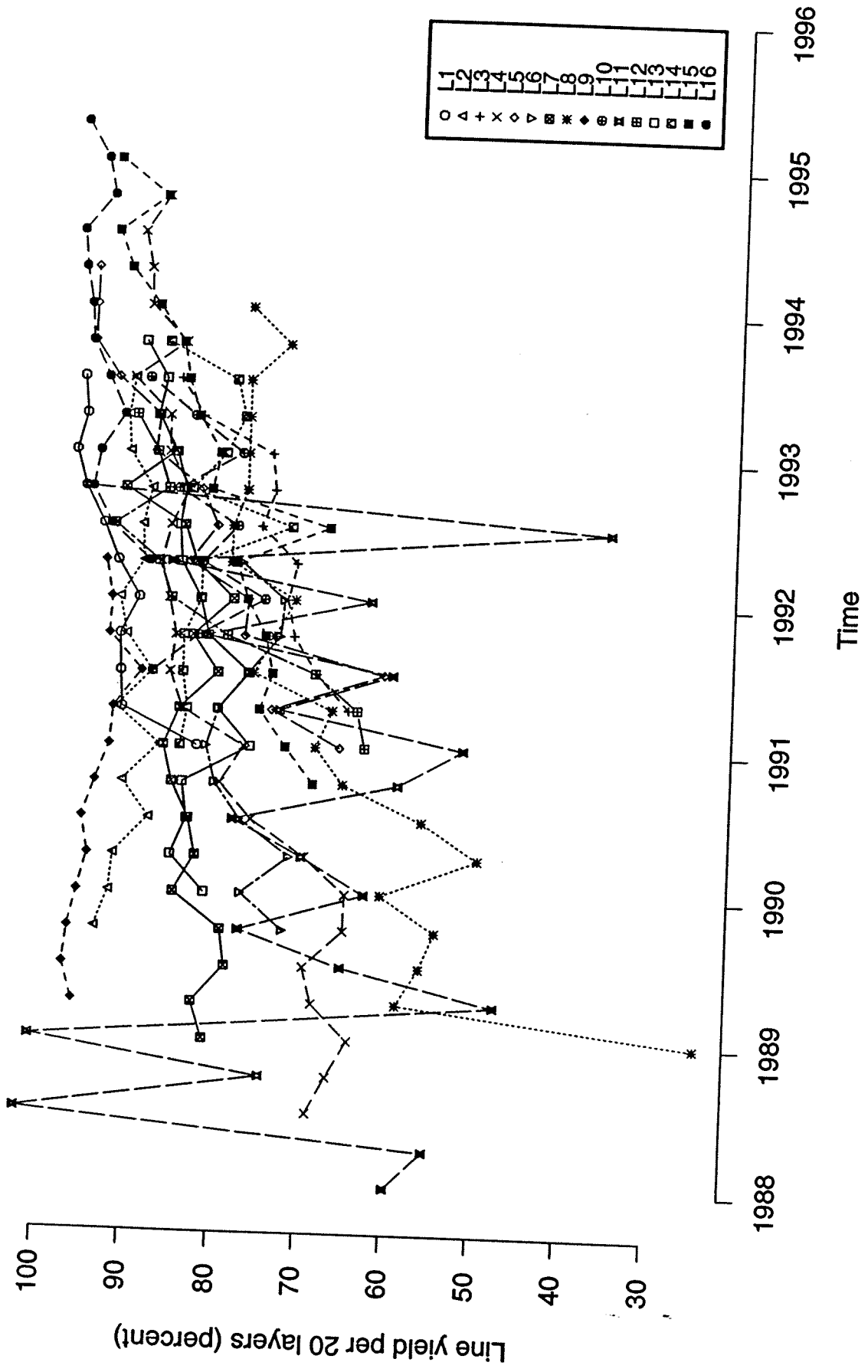
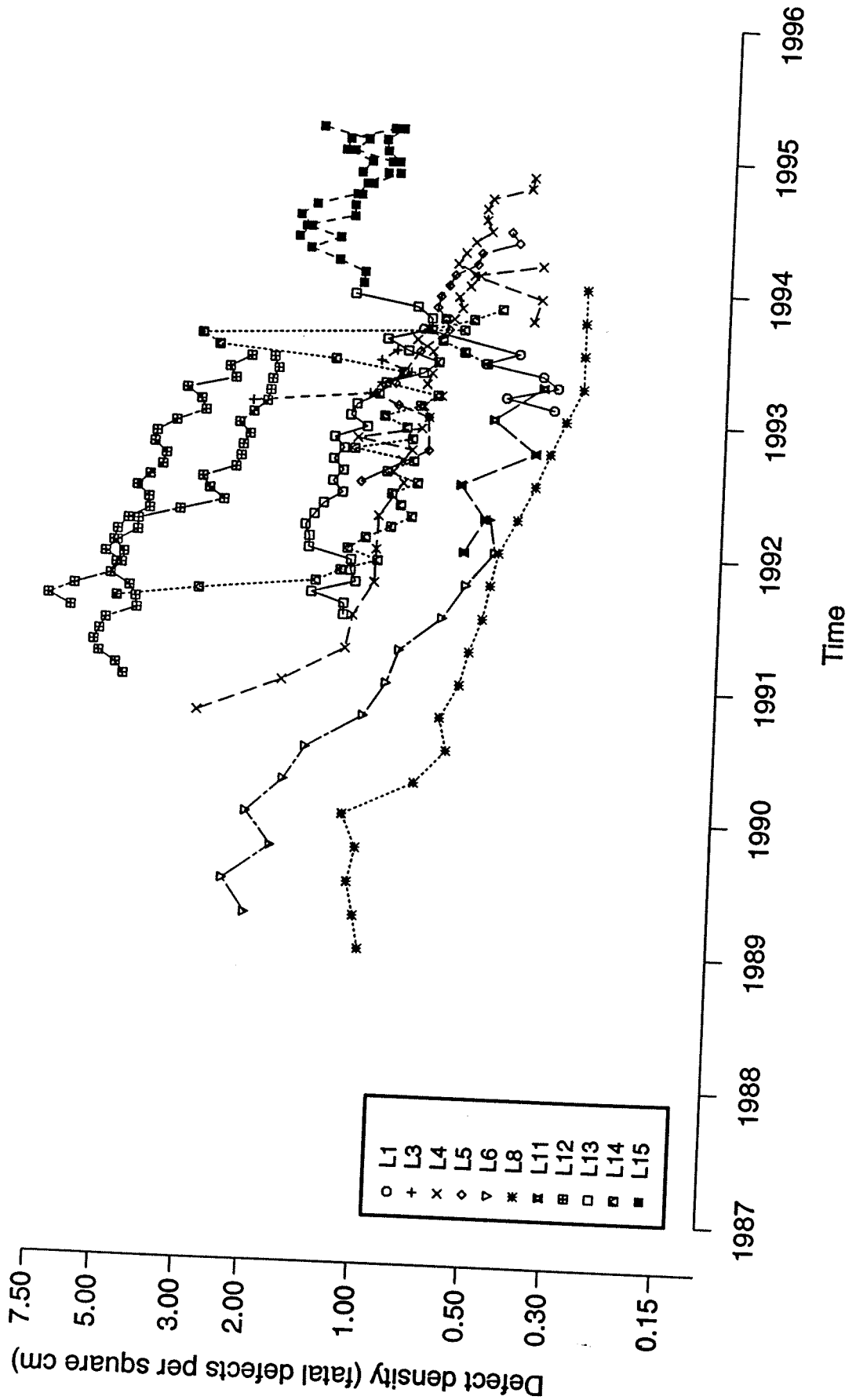


Figure 2.15. CMOS Logic Fab Line Yield

Figure 2.16. CMOS Logic Fab Defect Density

0.7 - 0.9 micron CMOS process flows



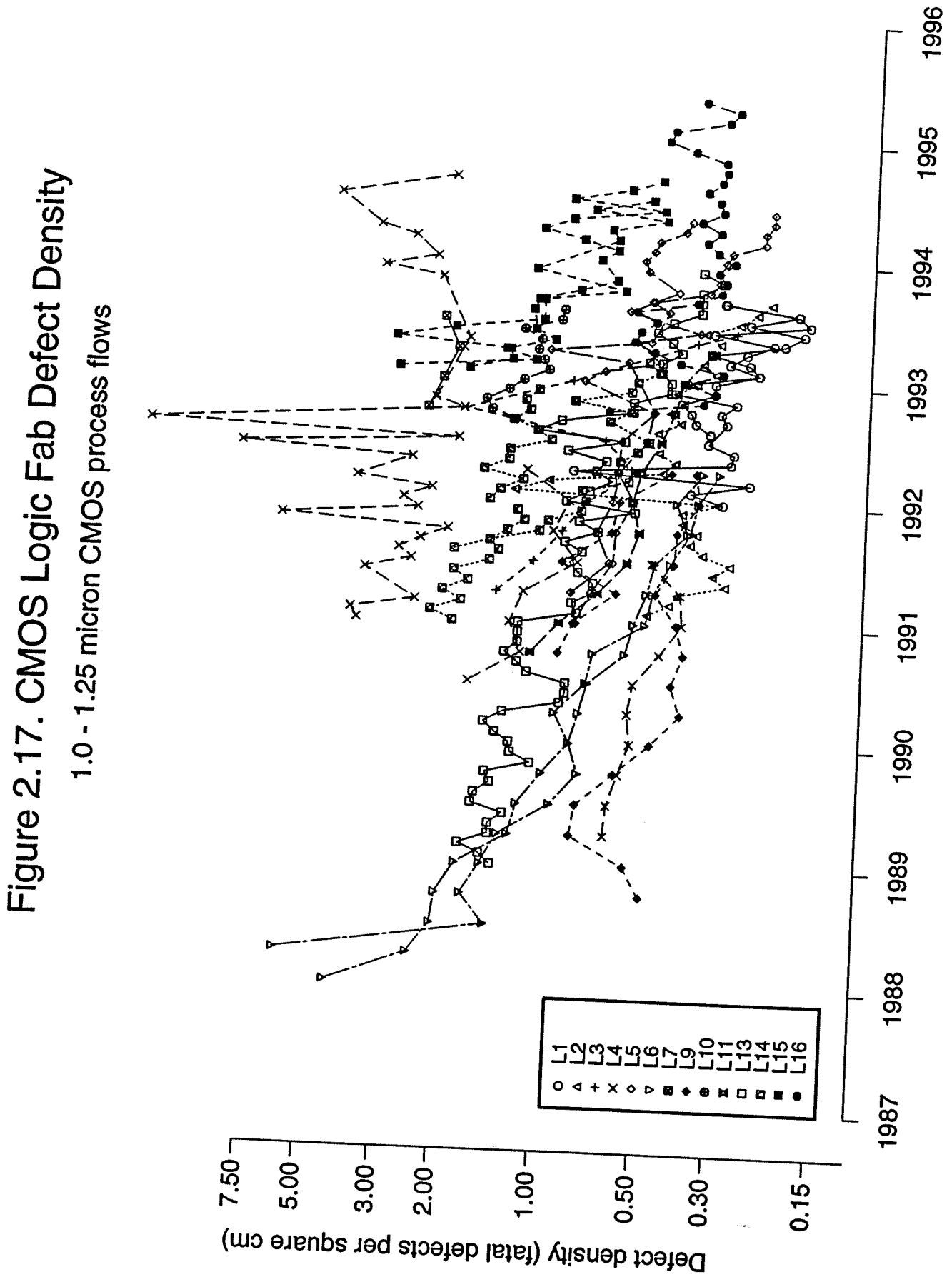


Figure 2.17. CMOS Logic Fab Defect Density
1.0 - 1.25 micron CMOS process flows
Defect density (fatal defects per square cm)
7.50
5.00
3.00
2.00
1.00
0.50
0.30
0.15
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time
L1
L2
L3
L4
L5
L6
L7
L9
L10
L11
L13
L14
L15
L16

Figure 2.18. CMOS Logic Fab Defect Density

1.3 - 1.5 micron CMOS process flows

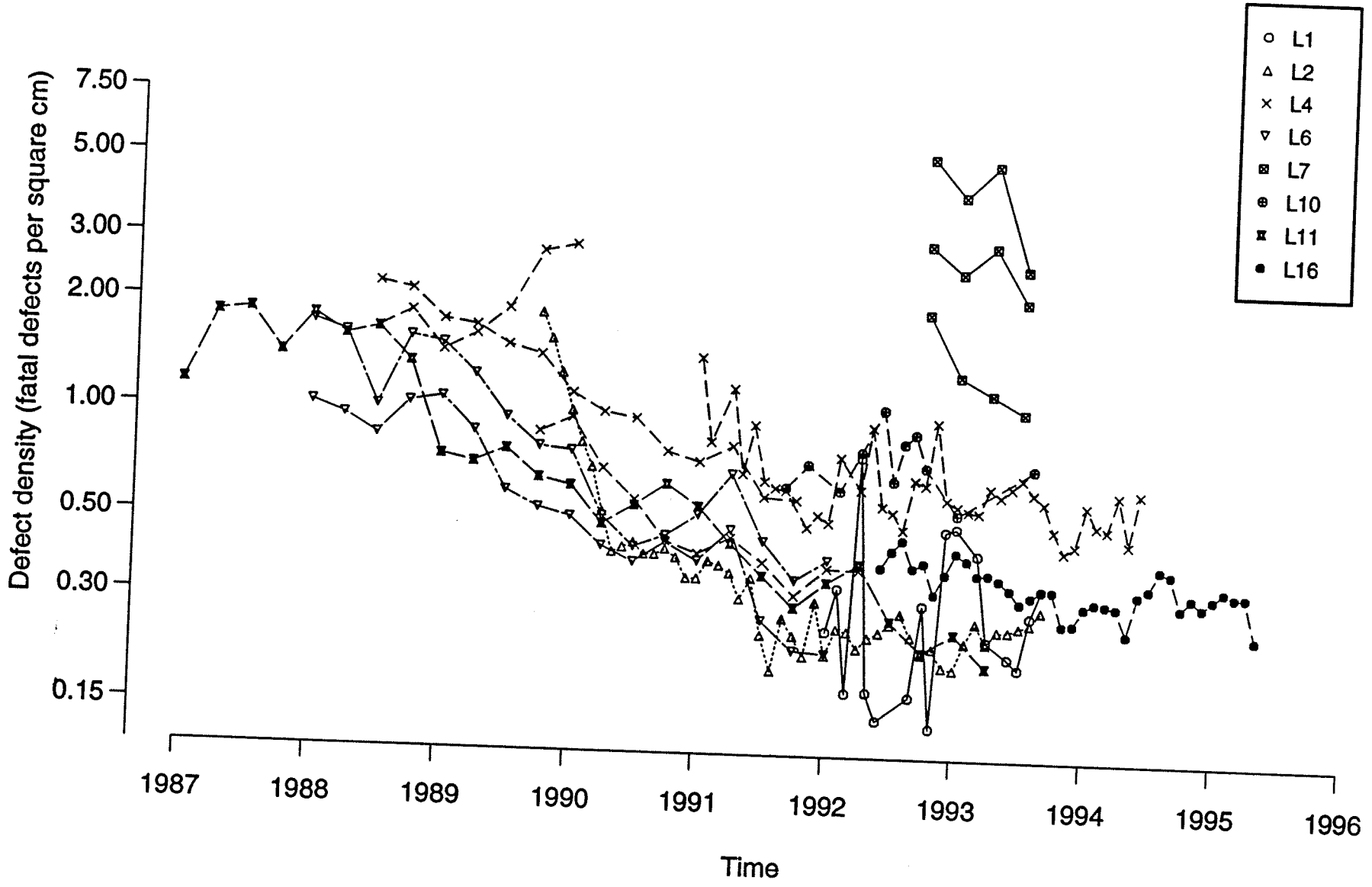
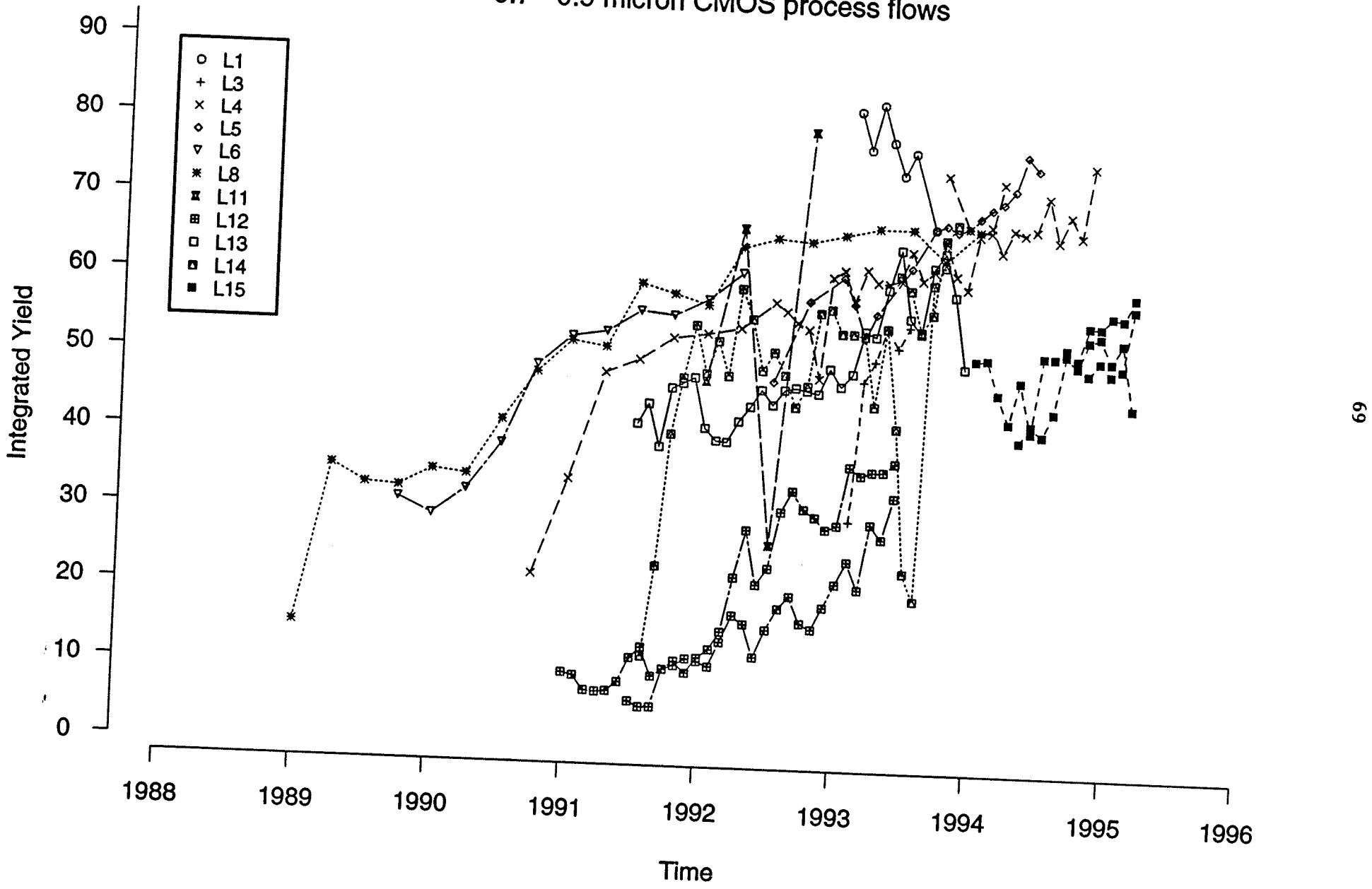


Figure 2.19. CMOS Logic Fab Integrated Yield

0.7 - 0.9 micron CMOS process flows



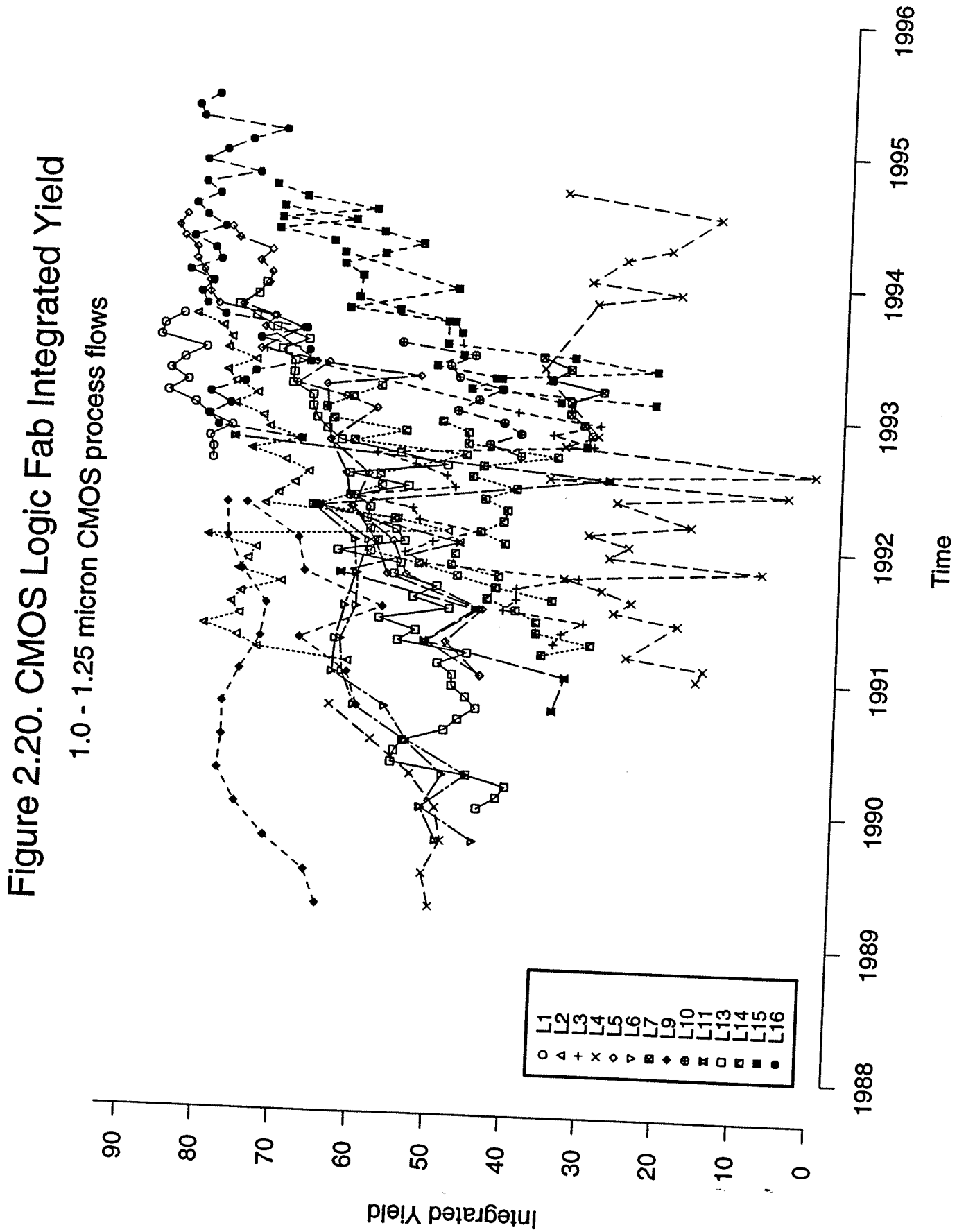


Figure 2.20. CMOS Logic Fab Integrated Yield
1.0 - 1.25 micron CMOS process flows
Integrated Yield
0
10
20
30
40
50
60
70
80
90
Time
1988
1989
1990
1991
1992
1993
1994
1995
1996
L1
L2
L3
L4
L5
L6
L7
L9
L10
L11
L13
L14
L15
L16

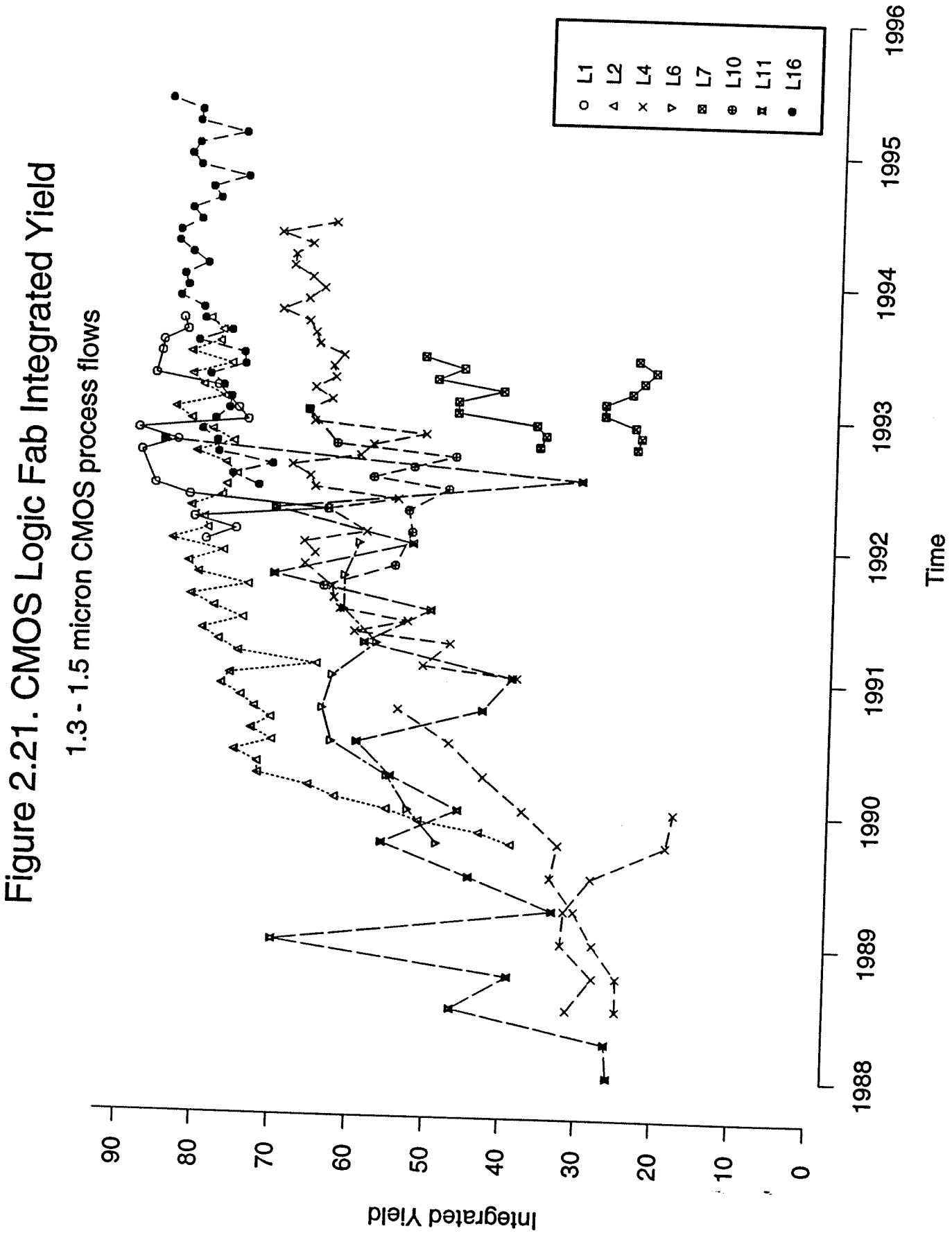


Figure 2.21. CMOS Logic Fab Integrated Yield
1.3 - 1.5 micron CMOS process flows
Integrated Yield
0
10
20
30
40
50
60
70
80
90
Time
1988
1989
1990
1991
1992
1993
1994
1995
1996
L1
L2
L4
L6
L7
L10
L11
L16

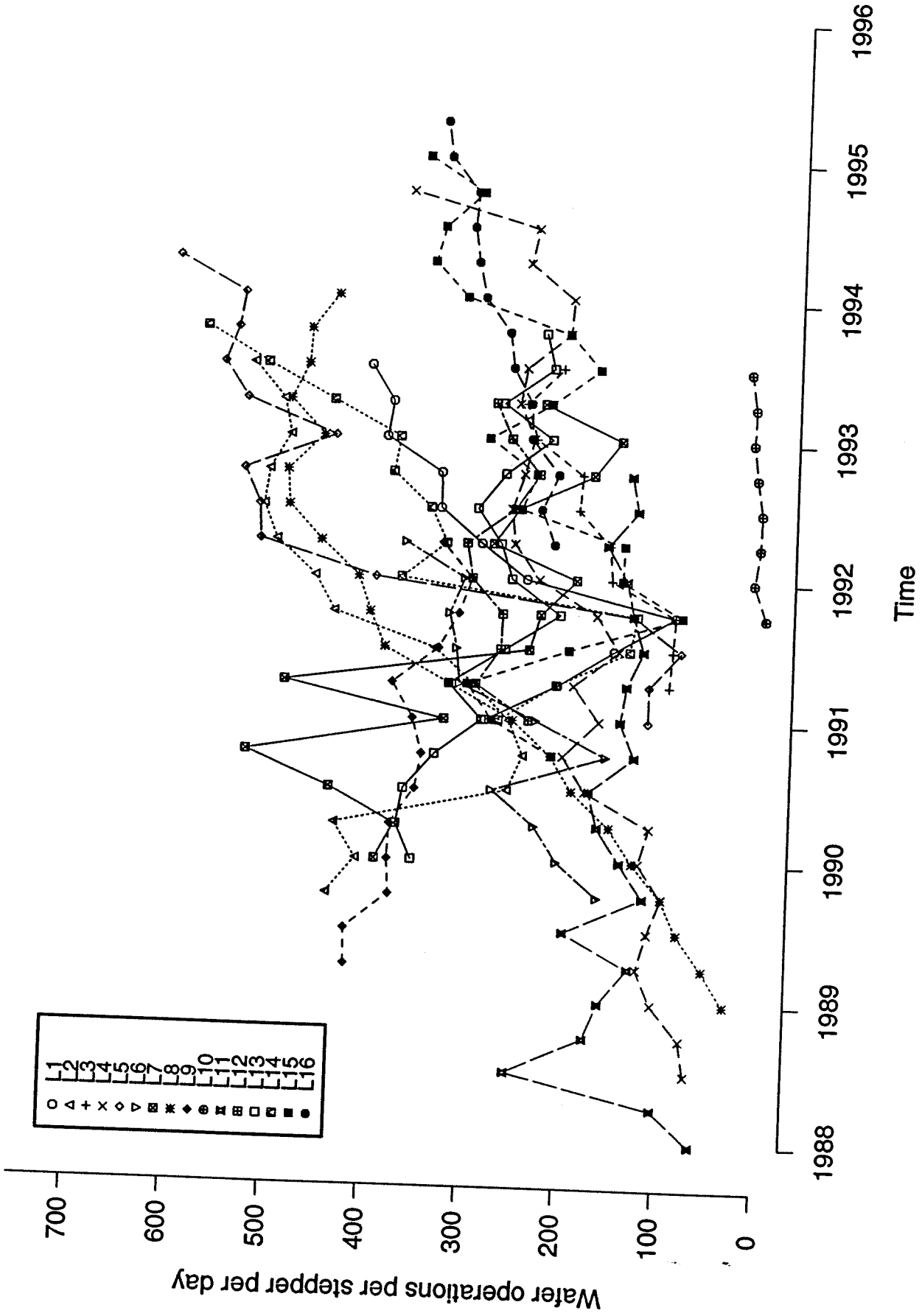


Figure 2.22. CMOS Logic Fab 5X Stepper Productivity
Wafer operations per stepper per day
0
100
200
300
400
500
600
700
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16

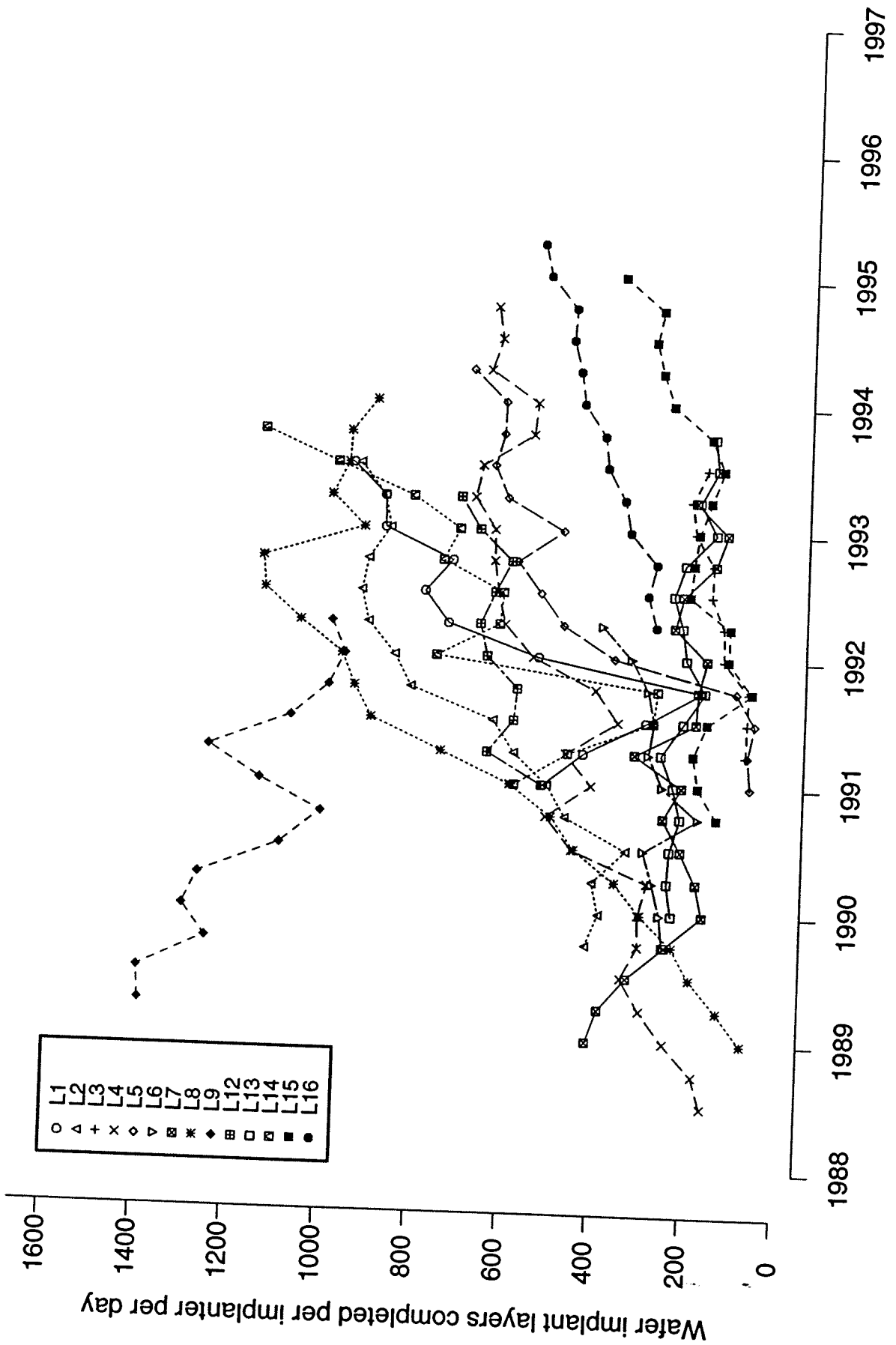


Figure 2.23. CMOS Logic Fab Ion Implanter Productivity
Wafer implant layers completed per implanter per day
1600
1400
1200
1000
800
600
400
200
0
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
Time
L1
L2
L3
L4
L5
L6
L7
L8
L9
L12
L13
L14
L15
L16

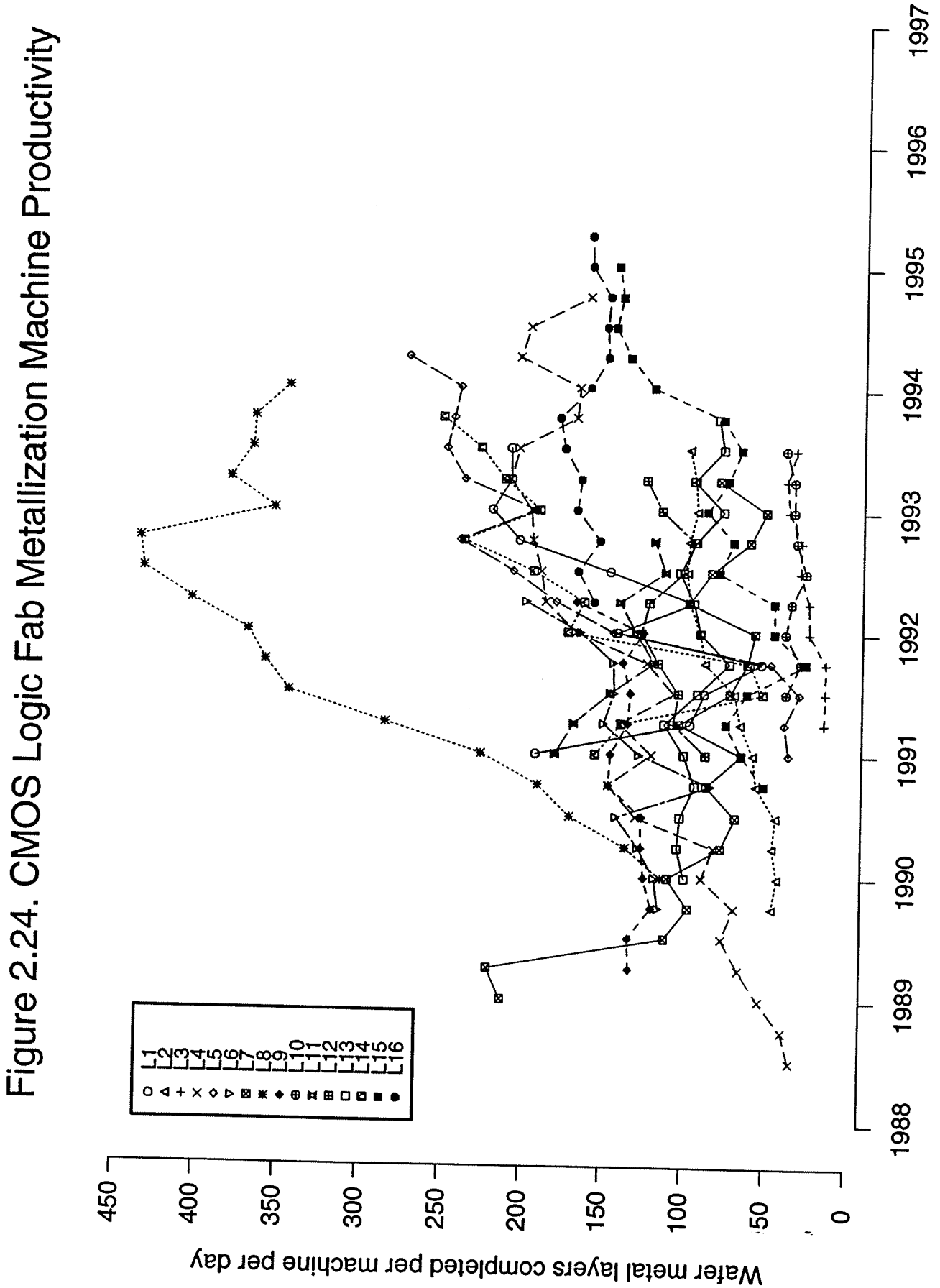
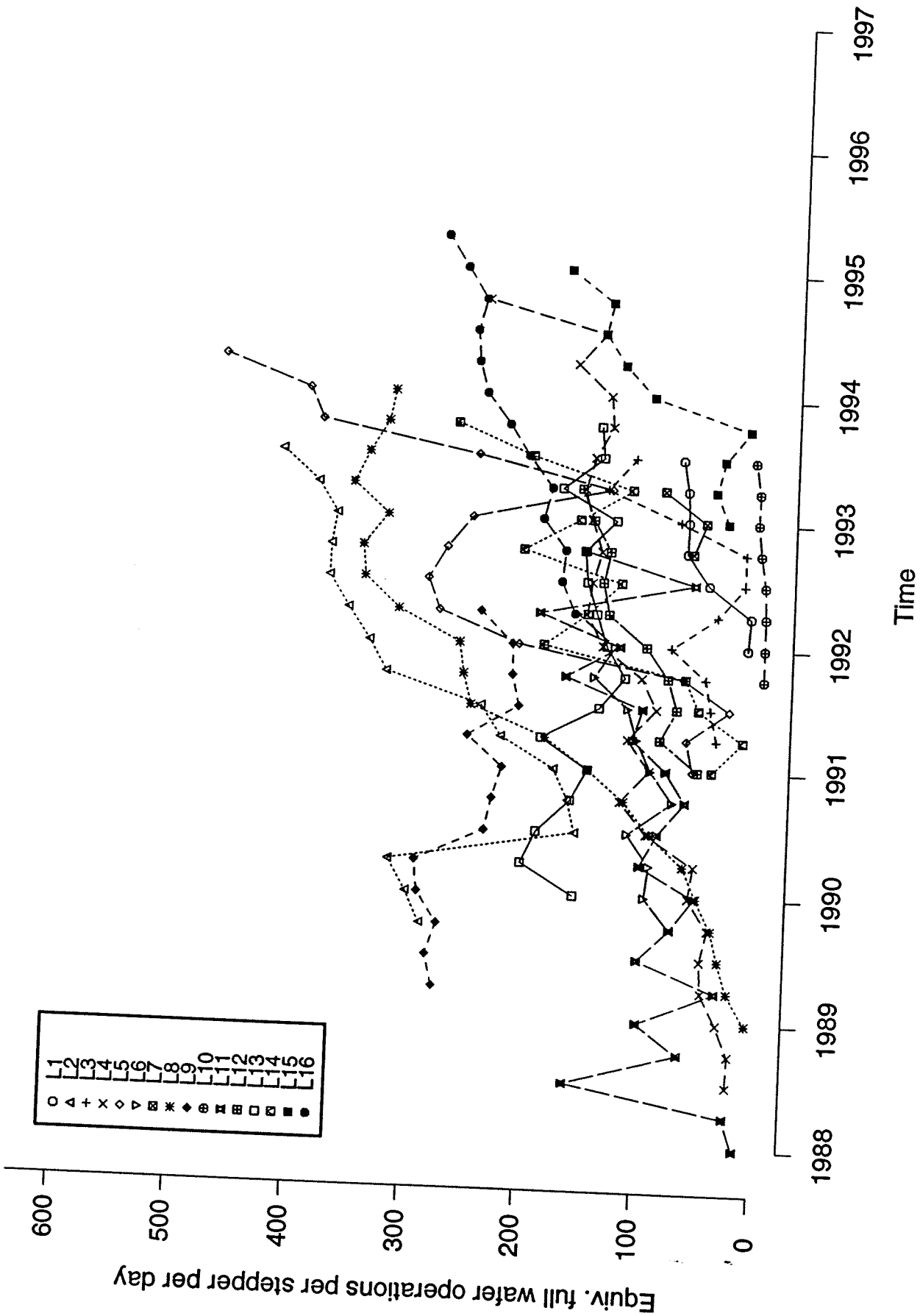


Figure 2.24. CMOS Logic Fab Metallization Machine Productivity
Wafer metal layers completed per machine per day
0
50
100
150
200
250
300
350
400
450
Time
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16

Figure 2.25. CMOS Logic Fab Integrated 5X Stepper Throughput



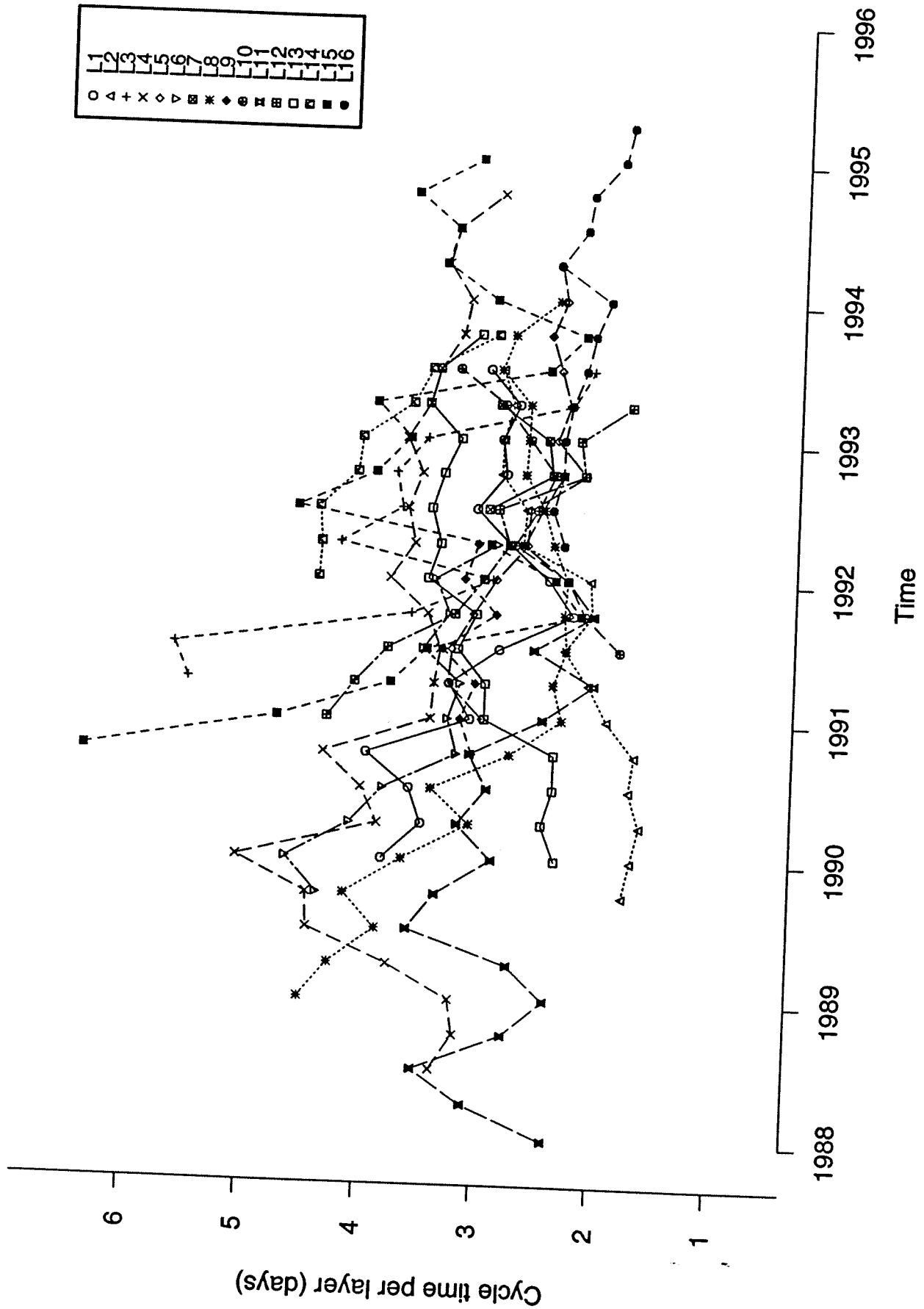


Figure 2.26. CMOS Logic Fab Cycle Time Per Layer
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
Cycle time per layer (days)
1
2
3
4
5
6
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time

Figure 2.27. CMOS Logic Fab Direct Labor Productivity

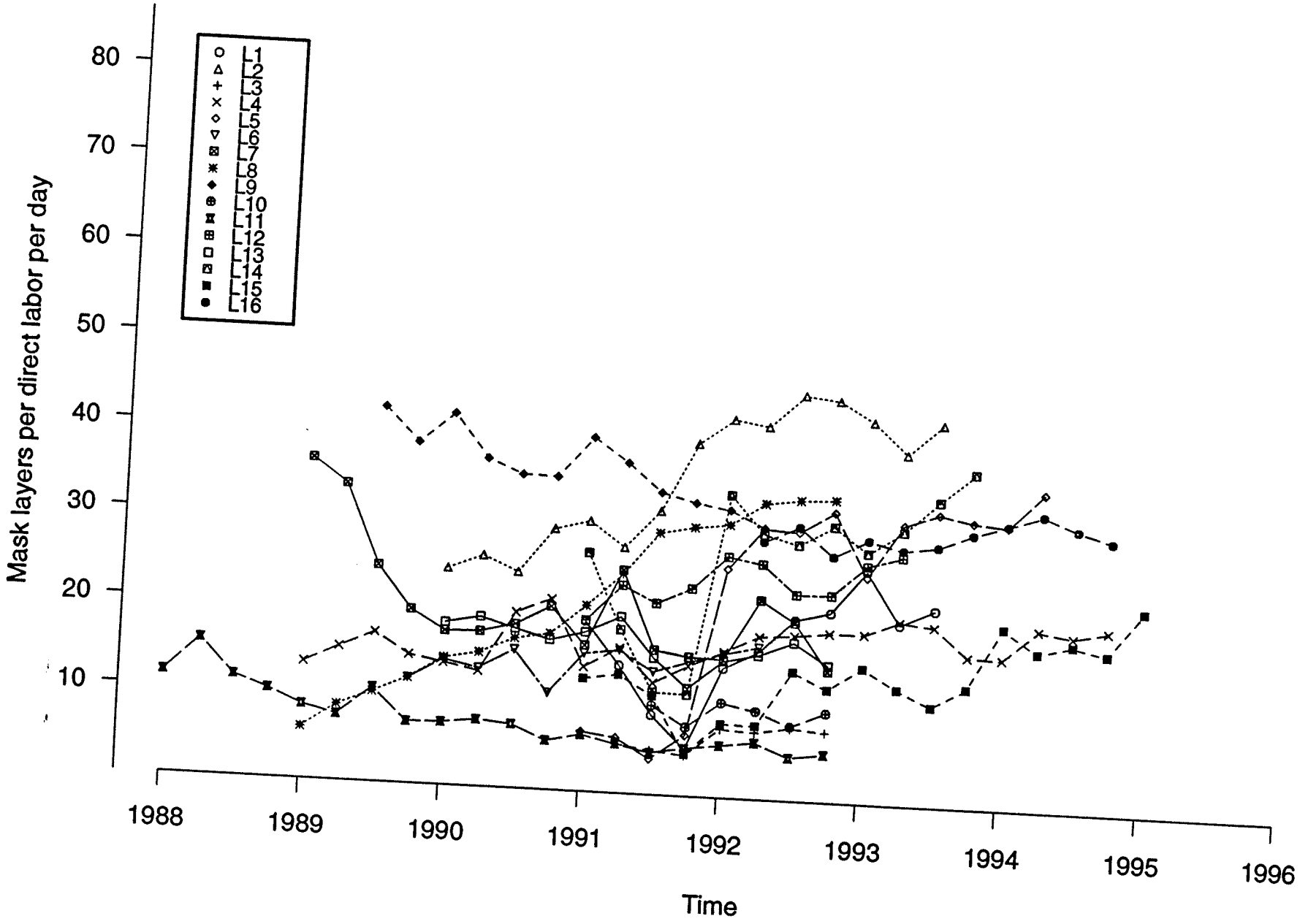


Figure 2.28. CMOS Logic Fab Total Labor Productivity

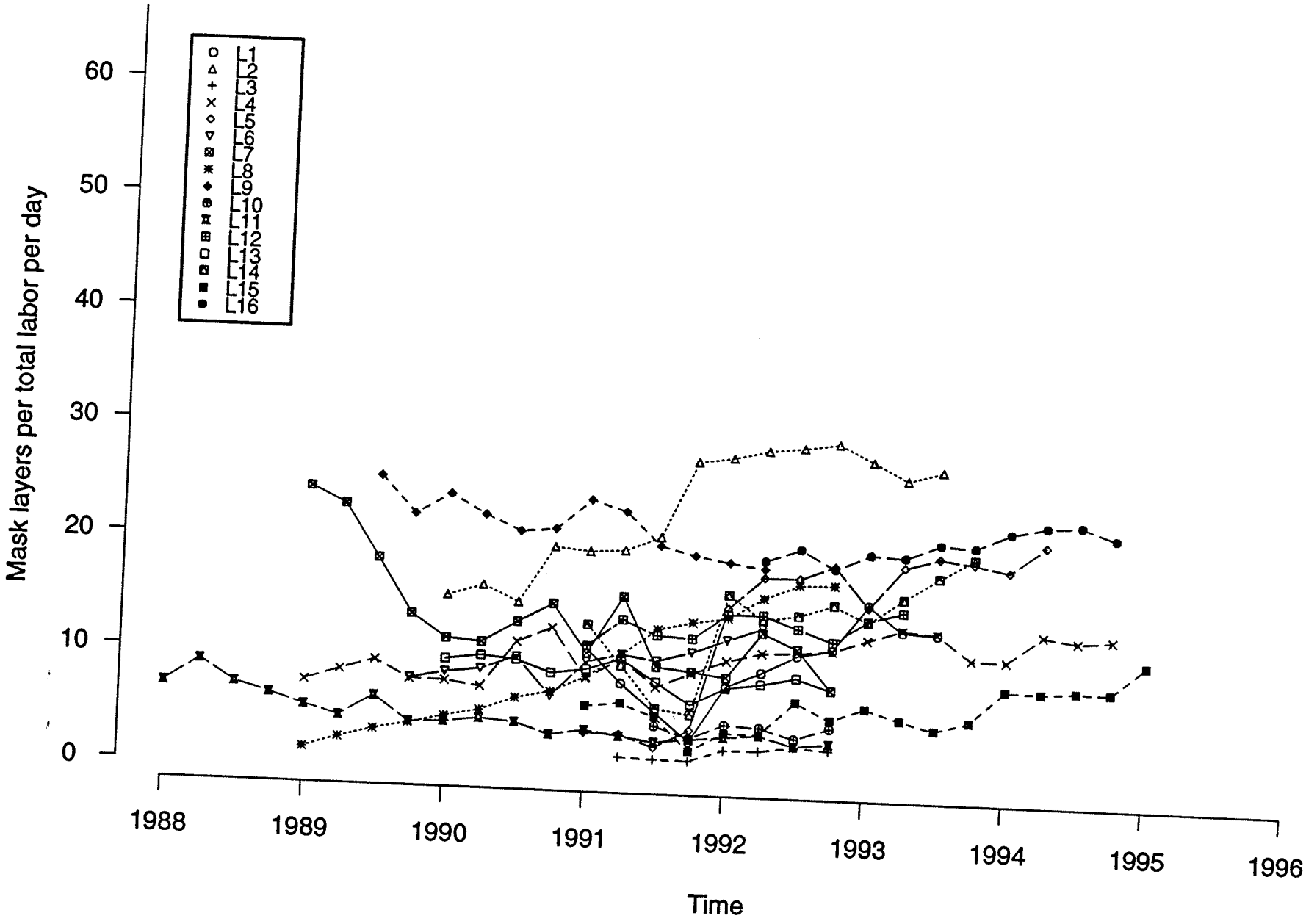


Table 2.18
CMOS Logic Fab Line Yields

Fab ID	Time	Line yield per 20 mask layers
L1	3Q93	96.6
L2	3Q93	90.9
L3	3Q93	85.6
L4	4Q94	87.7
L5	2Q94	95.4
L6	2Q92	78.1
L7	2Q93	88.0
L8	1Q94	77.8
L9	2Q92	93.5
L10	3Q93	89.2
L11	4Q92	95.8
L12	2Q93	90.5
L13	4Q93	89.8
L14	4Q93	87.1
L15	1Q95	93.2
L16	**2Q95**	**97.2**

Table 2.19
CMOS Logic Fab Defect Densities
0.7 - 0.9 micron CMOS process flows

Fab ID	Time	Murphy defect density
L1	3Q93	0.78
L3	2Q93	0.90
L4	1Q94	0.37
L5	2Q94	0.46
L6	2Q92	0.49
L8	**1Q94**	**0.28**
L11	**2Q93**	**0.28**
L12	2Q93	1.96
L13	4Q93	1.20
L14	4Q93	0.48
L15	1Q95	0.93

Table 2.20
CMOS Logic Fab Defect Densities
1.0 - 1.25 micron CMOS process flows

Fab ID	Time	Murphy defect density
L1	3Q93	0.31
L2	**3Q93**	**0.23**
L3	2Q93	0.29
L4	2Q92	1.19
L5	**2Q94**	**0.23**
L6	2Q92	0.32
L9	2Q92	0.37
L10	3Q93	0.96
L11	2Q93	0.24
L12	3Q93	2.16
L13	4Q93	0.37
L14	1Q93	0.53
L15	3Q94	0.50
L16	2Q95	0.38

Table 2.21
CMOS Logic Fab Defect Densities
1.3 - 1.5 micron CMOS process flows

Fab ID	Time	Murphy defect density
L1	3Q93	0.34
L2	3Q93	0.30
L4	2Q92	0.38
L6	1Q92	0.22
L10	3Q93	0.74
L11	**2Q93**	**0.14**
L12	3Q93	1.07
L16	2Q95	0.26

Table 2.22
CMOS Logic Fab Integrated Yields
0.7 - 0.9 micron CMOS process flows

Fab ID	Time	Integrated line and die yield (0.5 sq cm die)
L1	3Q93	66.8
L3	3Q93	55.2
L4	4Q94	76.4
L5	2Q94	75.8
L6	2Q92	61.5
L8	1Q94	67.7
L11	**4Q92**	**83.0**
L12	2Q93	37.8
L13	4Q93	50.2
L14	4Q93	68.5
L15	1Q95	59.8

Table 2.23
CMOS Logic Fab Integrated Yields
1.0 - 1.25 micron CMOS process flows

Fab ID	Time	Integrated line and die yield (0.5 sq cm die)
L1	**3Q93**	**84.6**
L2	3Q93	82.9
L3	2Q93	73.6
L4	4Q90	63.9
L5	**2Q94**	**84.6**
L6	2Q92	66.8
L9	2Q92	78.0
L10	3Q93	56.0
L11	4Q92	82.1
L12	2Q93	37.5
L13	4Q93	73.9
L14	1Q93	58.6
L15	3Q94	71.9
L16	2Q95	81.0

Table 2.24
CMOS Logic Fab Integrated Yields
1.3 - 1.5 micron CMOS process flows

Fab ID	Time	Integrated line and die yield (0.5 sq cm die)
L1	3Q93	83.5
L2	3Q93	80.1
L4	2Q94	64.0
L6	1Q92	60.0
L10	4Q92	63.2
L11	4Q92	85.7
L12	2Q93	52.1
L16	**2Q95**	**85.9**

Table 2.25
CMOS Logic Fab 5X Stepper Throughput

Fab ID	Time	Wafer operations per 5X stepper per day
L1	3Q93	408
L2	3Q93	528
L3	3Q93	213
L4	4Q94	372
L5	**2Q94**	**606**
L6	2Q92	369
L7	2Q93	231
L8	1Q94	444
L9	2Q92	331
L10	3Q93	21
L11	4Q92	140
L12	2Q93	281
L13	4Q93	232
L14	4Q93	575
L15	1Q95	356
L16	2Q95	340

Table 2.26
CMOS Logic Fab Ion Implanter Throughput

Fab ID	Time	Wafer operations per implanter per day
L1	3Q93	955
L2	3Q93	940
L3	3Q93	179
L4	4Q94	648
L5	2Q94	698
L6	2Q92	397
L7	2Q93	201
L8	1Q94	907
L9	2Q92	992
L12	2Q93	718
L13	4Q93	163
L14	**4Q93**	**1146**
L15	1Q95	369
L16	2Q95	549

Table 2.27
CMOS Logic Fab Metallization Machine Throughput

Fab ID	Time	Wafer operations per machine per day
L1	3Q93	210
L2	3Q93	99
L3	3Q93	34
L4	4Q94	162
L5	2Q94	273
L7	2Q93	80
L8	**1Q95**	**345**
L9	2Q92	169
L10	3Q93	40
L11	4Q92	120
L12	2Q93	136
L13	4Q93	82
L14	4Q93	252
L15	1Q95	145
L16	2Q95	162

Table 2.28
CMOS Logic Fab Integrated 5X Stepper Throughput

Fab ID	Time	Equiv. full wafer operations per 5X stepper per day
L1	3Q93	75
L2	3Q93	419
L3	3Q93	115
L4	4Q94	245
L5	**2Q94**	**469**
L6	2Q92	161
L7	2Q93	59
L8	1Q94	323
L9	2Q92	244
L10	3Q93	12
L11	4Q92	155
L12	2Q93	160
L13	4Q93	145
L14	4Q93	269
L15	1Q95	175
L16	2Q95	283

Table 2.29
CMOS Logic Fab Cycle Time

Fab ID	Time	Cycle time per mask layer
L1	3Q93	3.0
L2	3Q93	2.9
L3	3Q93	2.1
L4	4Q94	3.0
L5	2Q94	2.4
L6	2Q92	2.9
L7	4Q92	2.5
L8	1Q94	2.5
L9	2Q92	3.1
L10	3Q93	3.3
L11	4Q94	2.4
L12	**2Q93**	**1.8**
L13	4Q93	3.1
L14	4Q93	2.9
L15	1Q95	3.2
L16	2Q95	1.9

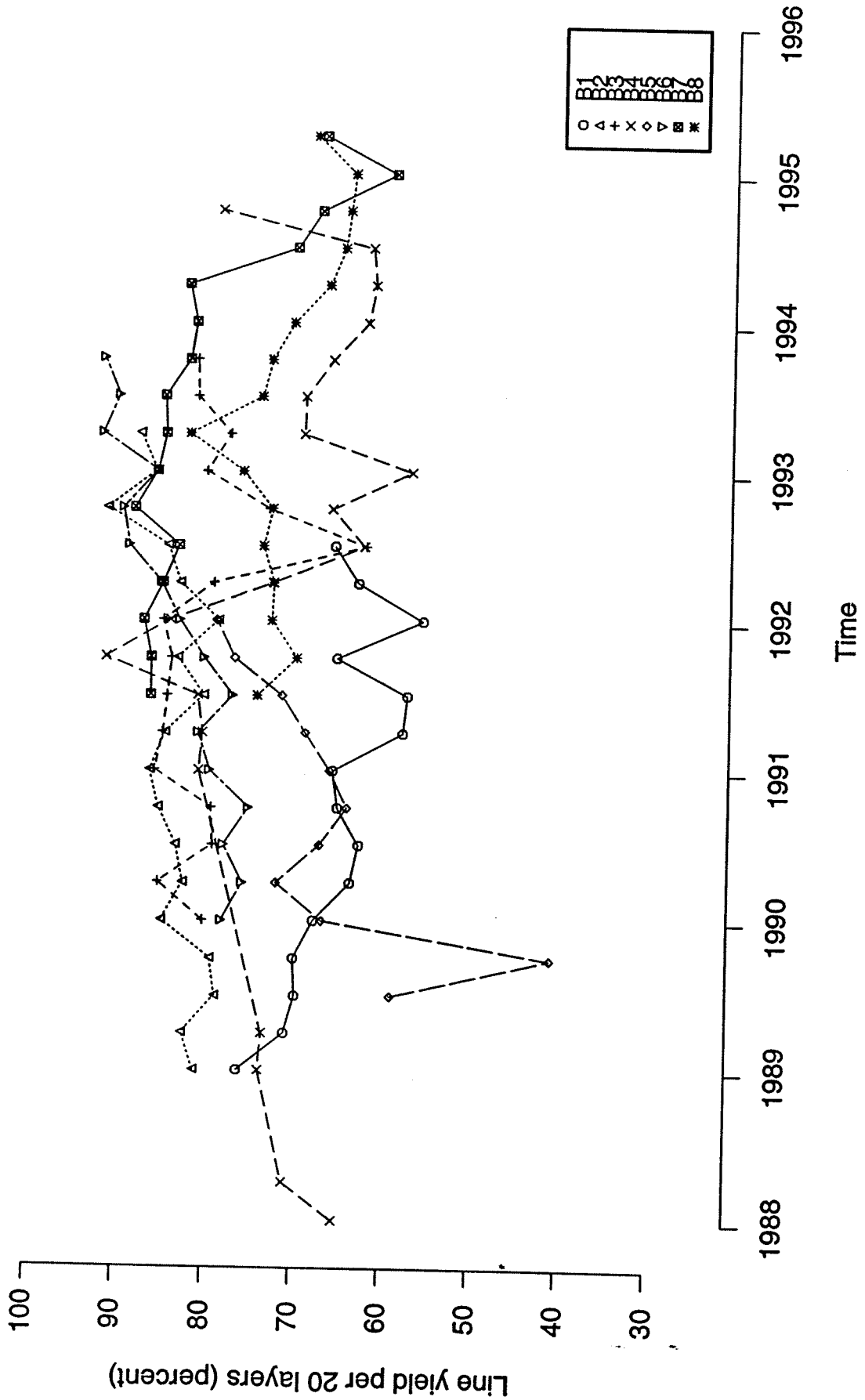
Table 2.30
CMOS Logic Fab Direct Labor Productivity

Fab ID	Time	Wafer mask layers completed per operator per day
L1	3Q93	22.3
L2	**3Q93**	**43.4**
L3	4Q92	8.0
L4	4Q94	20.7
L5	2Q94	36.1
L6	2Q92	17.2
L7	4Q92	15.8
L8	4Q92	34.3
L9	2Q92	30.8
L10	4Q92	10.1
L11	4Q92	5.5
L12	2Q93	28.1
L13	4Q92	15.5
L14	4Q93	38.0
L15	1Q95	23.1
L16	4Q94	30.9

Table 2.31
CMOS Logic Fab Total Labor Productivity

Fab ID	Time	Wafer mask layers completed per person per day
L1	3Q93	26.8
L2	**3Q93**	**27.6**
L3	4Q92	2.7
L4	4Q94	13.2
L5	2Q94	21.3
L6	2Q92	13.2
L7	4Q92	8.0
L8	4Q92	17.3
L9	2Q92	18.5
L10	4Q92	4.7
L11	4Q92	3.3
L12	2Q93	15.1
L13	4Q92	8.0
L14	4Q93	20.0
L15	1Q95	11.1
L16	4Q94	22.2

Figure 2.29. MSI Fab Line Yield



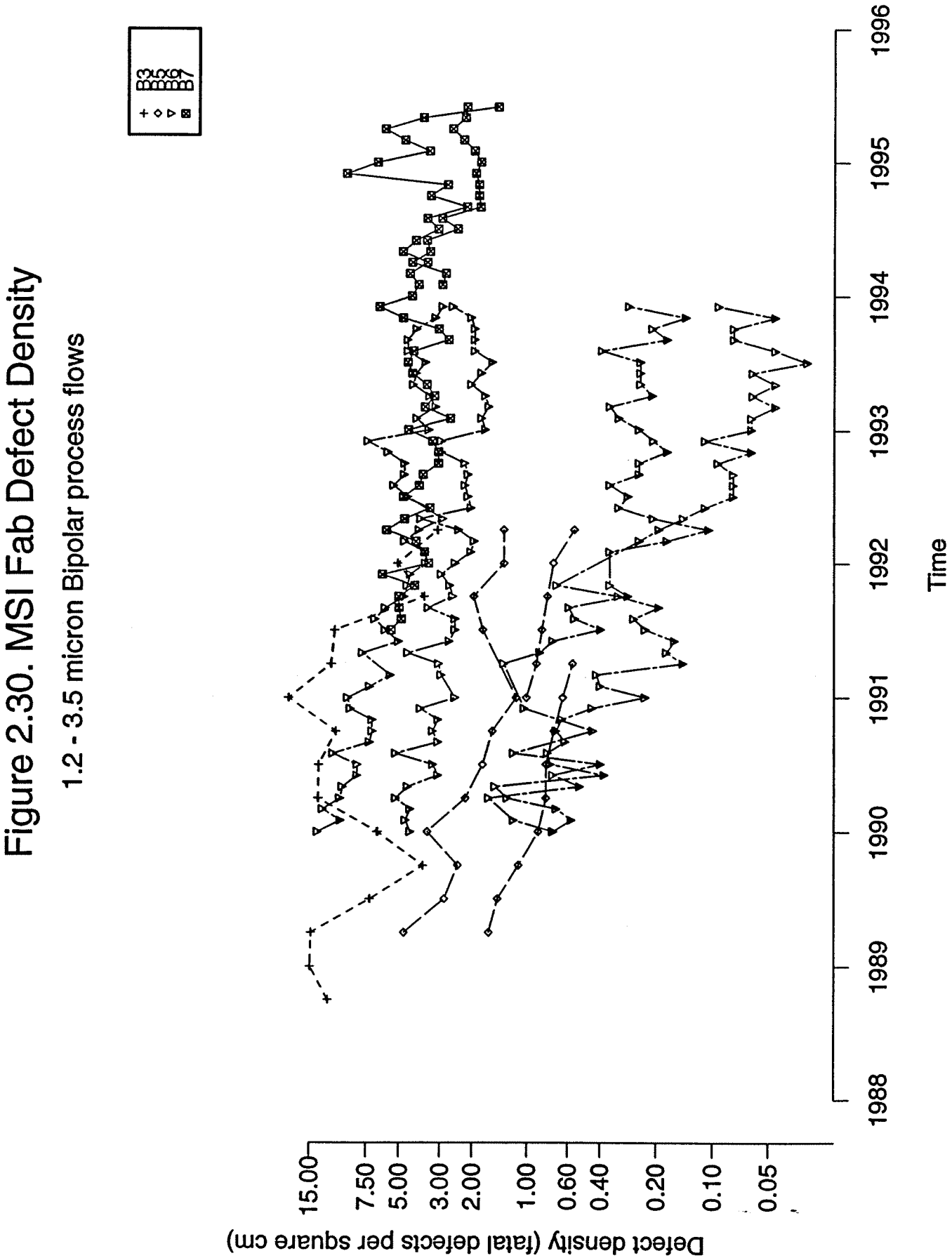


Figure 2.30. MSI Fab Defect Density
1.2 - 3.5 micron Bipolar process flows
B3
B5
B6
B7
Defect density (fatal defects per square cm)
15.00
7.50
5.00
3.00
2.00
1.00
0.60
0.40
0.20
0.10
0.05
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time

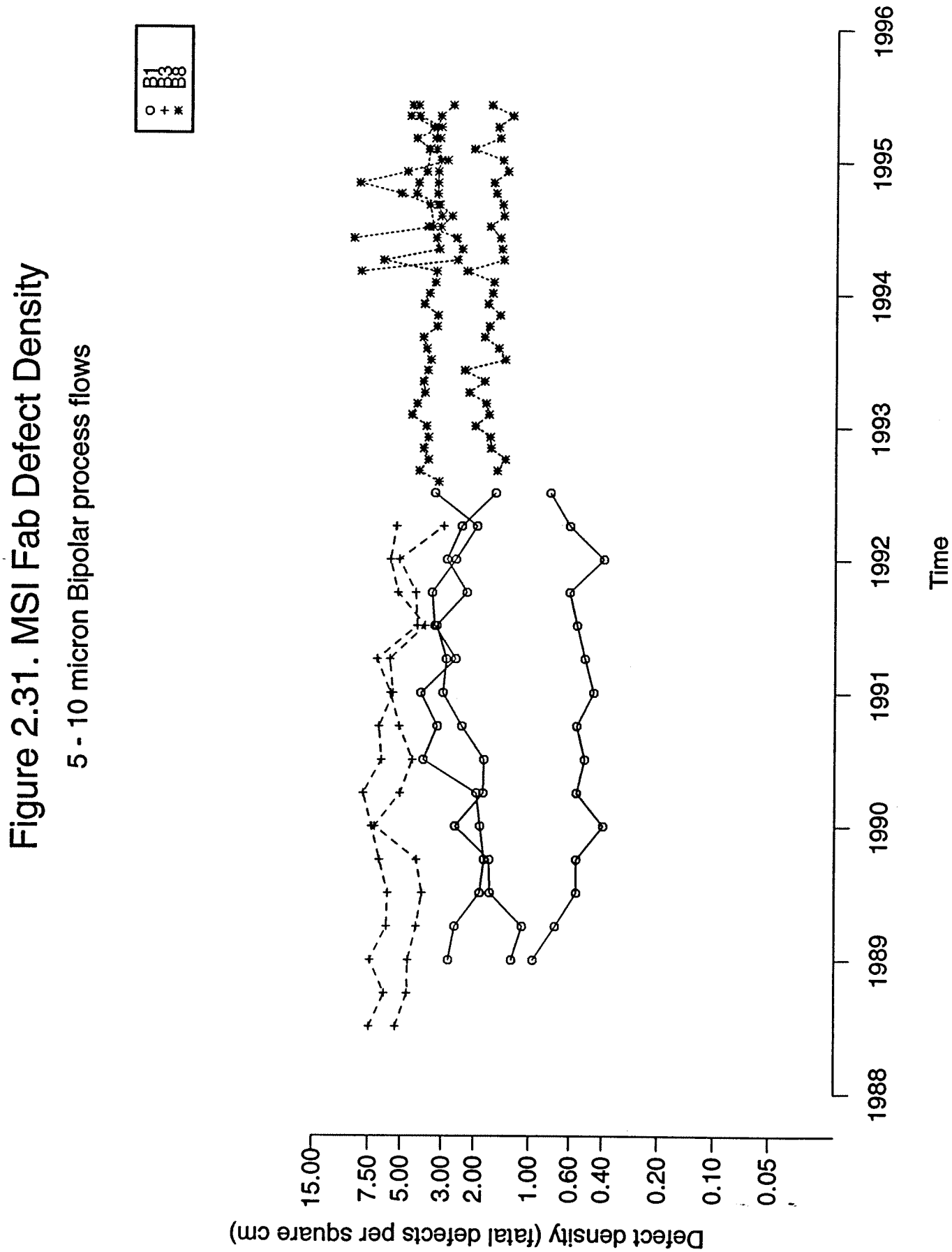


Figure 2.31. MSI Fab Defect Density

5 - 10 micron Bipolar process flows

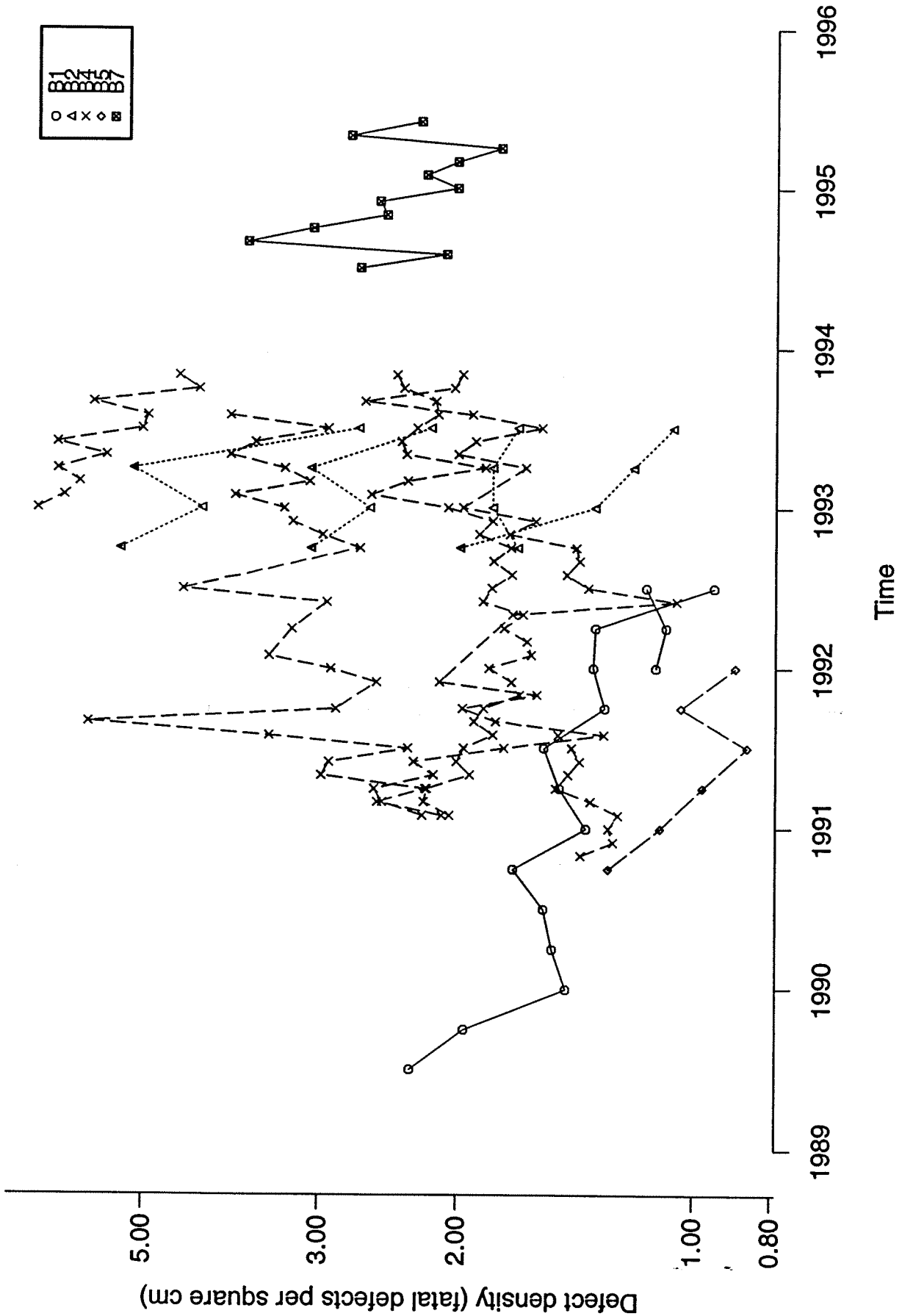


Figure 2.32. MSI Fab Defect Density

1.5 - 4.0 micron CMOS or BiCMOS process flows

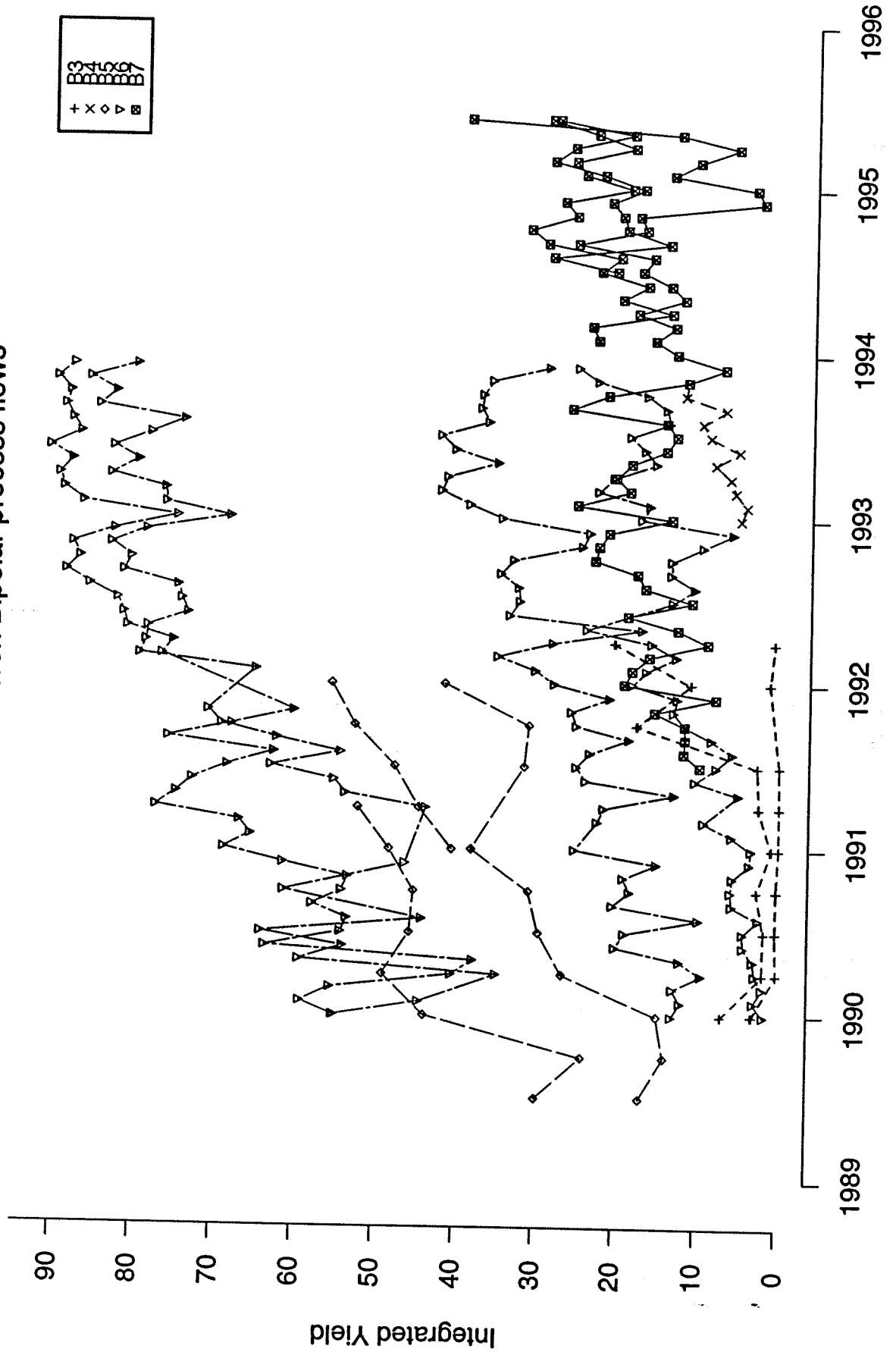


Figure 2.33. MSI Fab Integrated Yield

1.2 - 3.5 micron Bipolar process flows

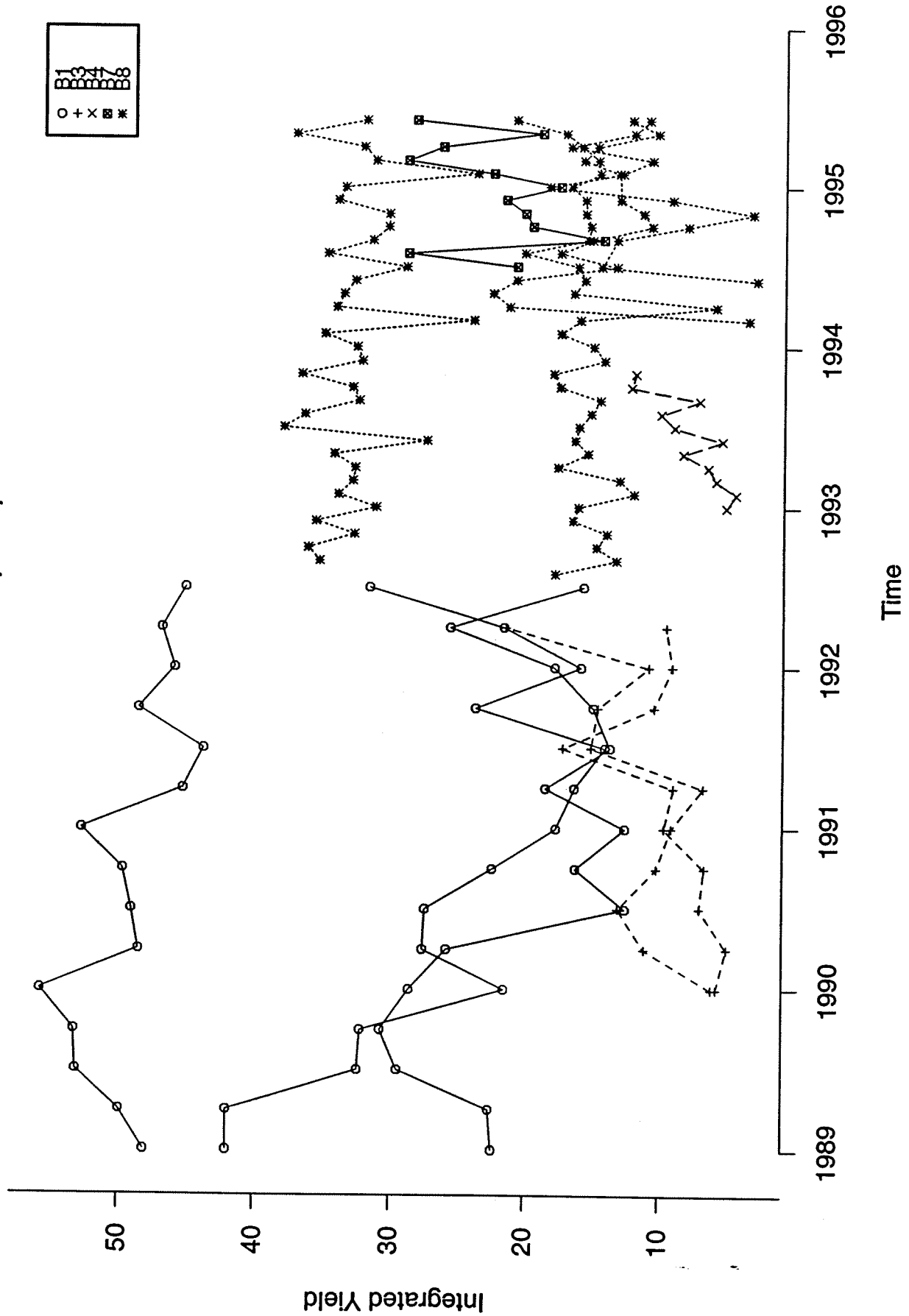


Figure 2.34. MSI Fab Integrated Yield

5.0 - 10.0 micron Bipolar process flows

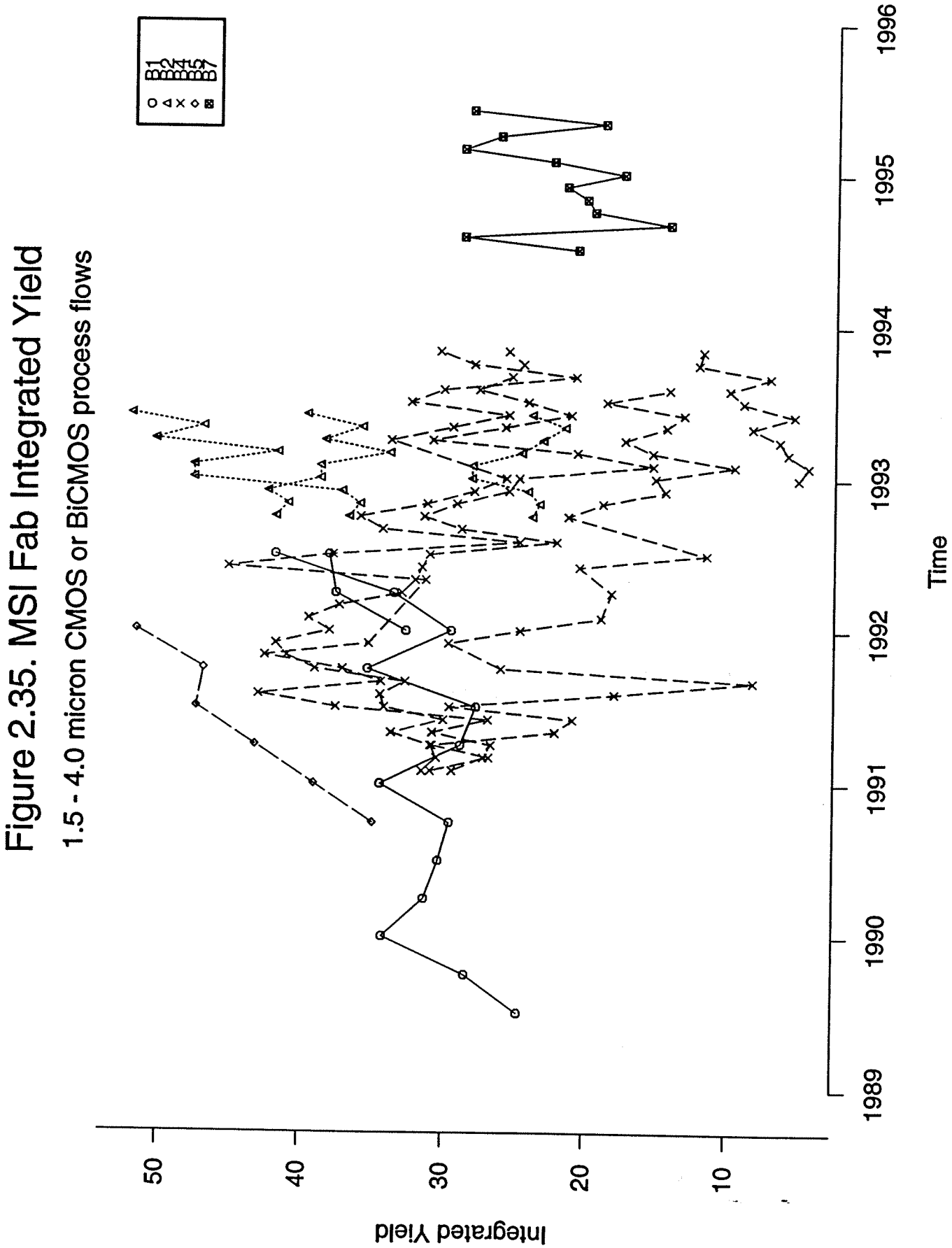


Figure 2.35. MSI Fab Integrated Yield
1.5 - 4.0 micron CMOS or BiCMOS process flows
B1
B2
B4
B5
B7
Integrated Yield
50
40
30
20
10
1989
1990
1991
1992
1993
1994
1995
1996
Time

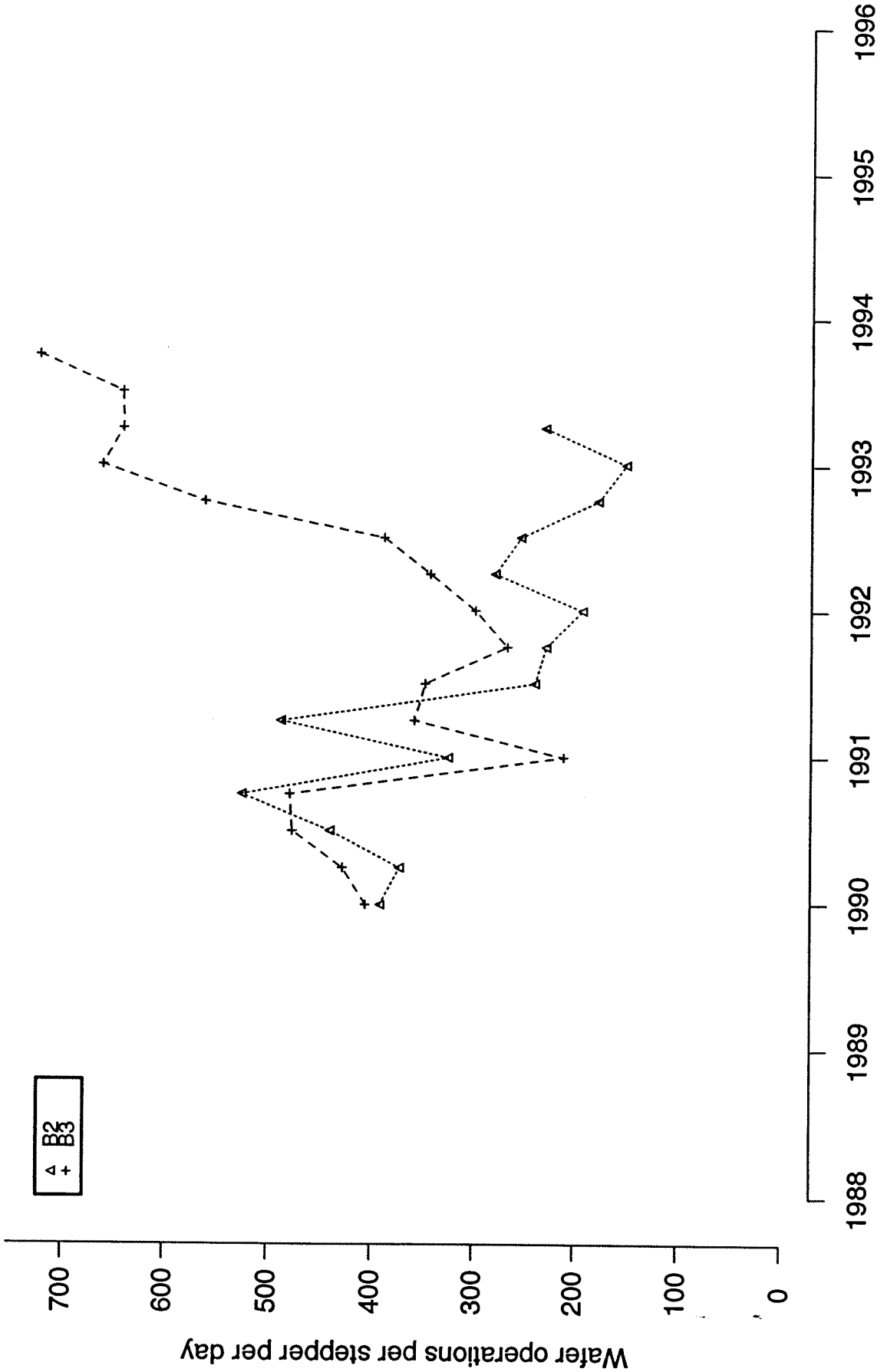
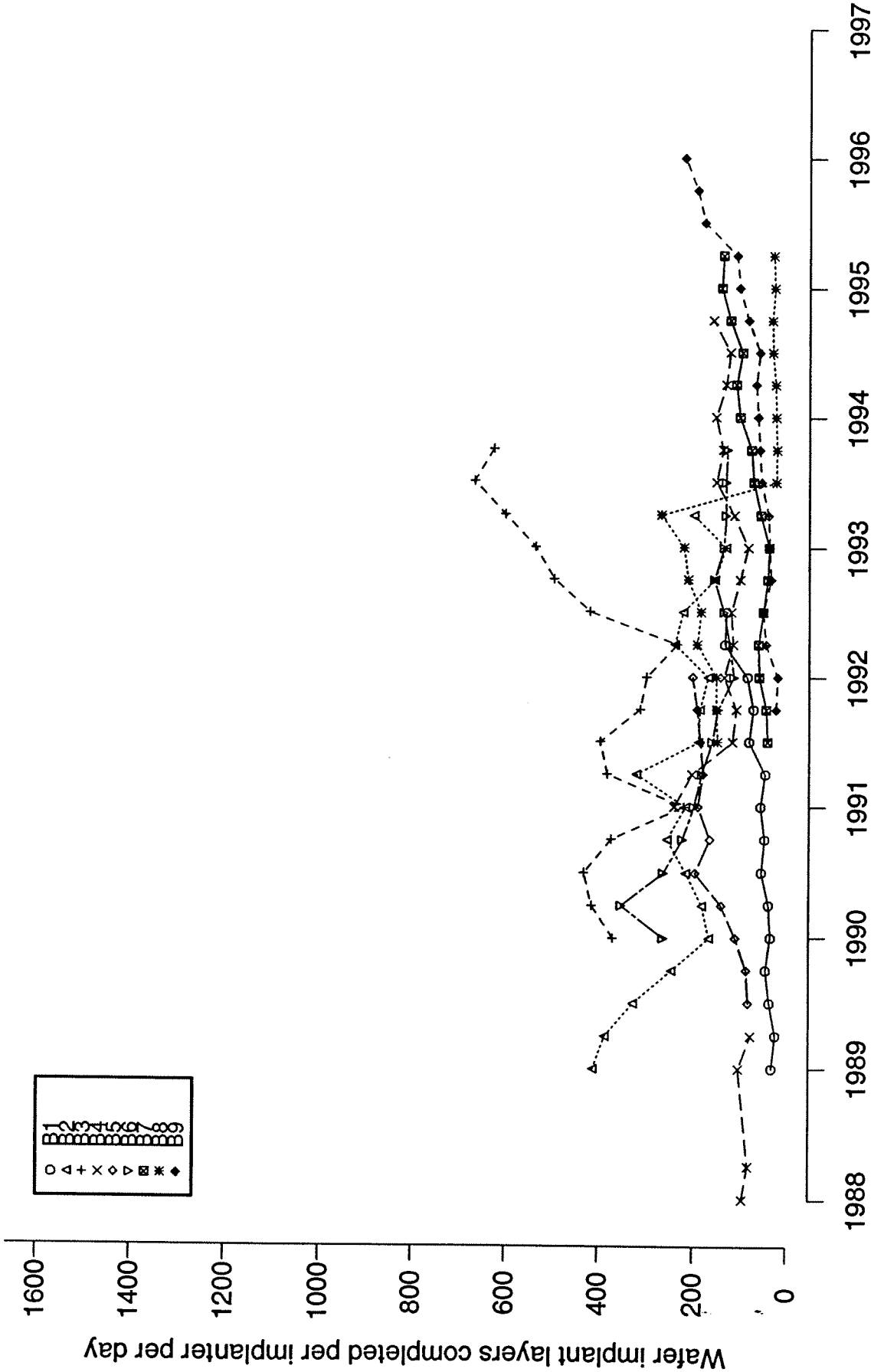


Figure 2.36. MSI Fab 5X Stepper Productivity
B2
B3
Wafer operations per stepper per day
0
100
200
300
400
500
600
700
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time

Figure 2.37. MSI Fab Ion Implanter Productivity



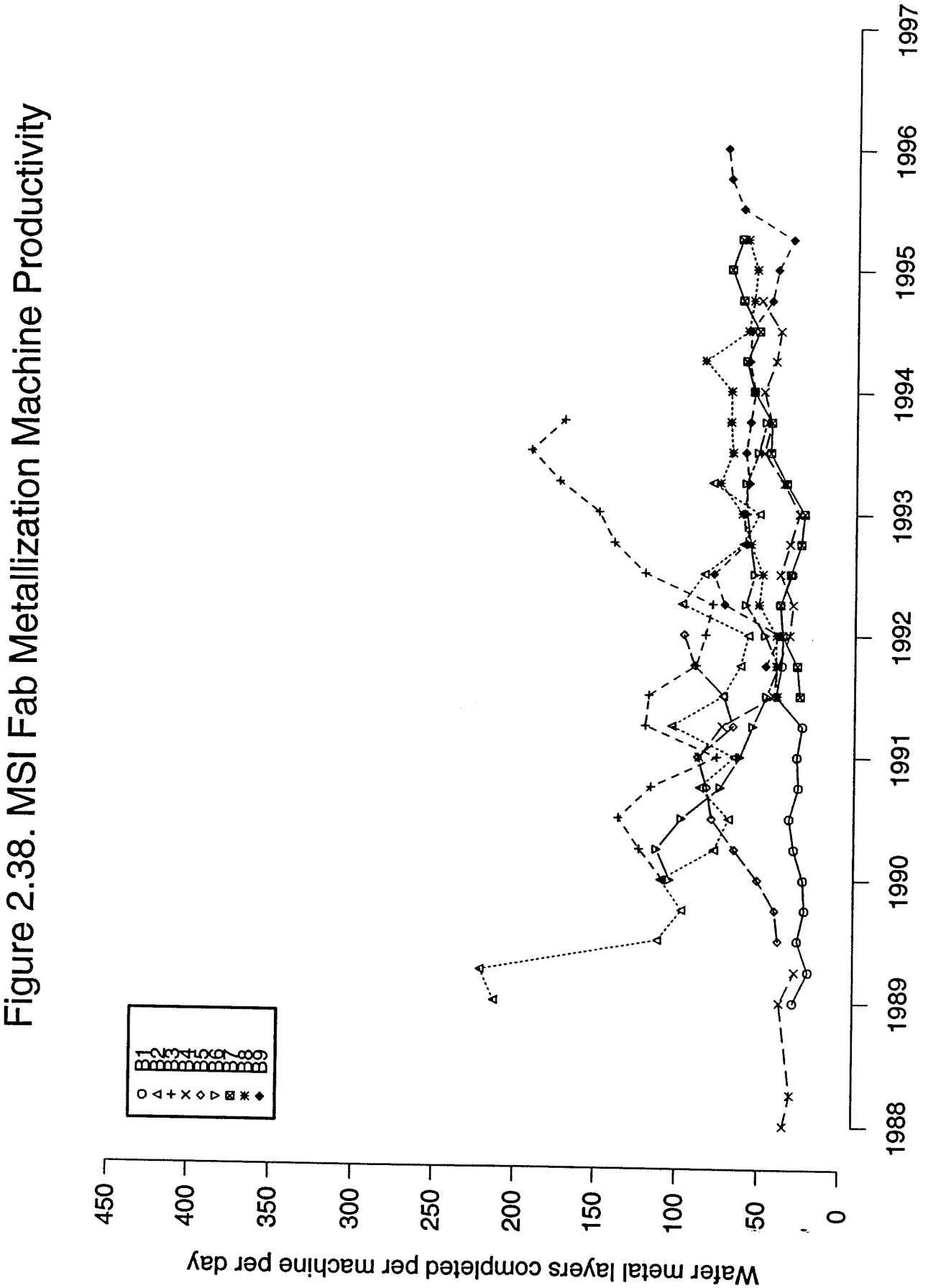


Figure 2.38. MSI Fab Metallization Machine Productivity
Wafer metal layers completed per machine per day
450
400
350
300
250
200
150
100
50
0
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
Time
B1
B2
B3
B4
B5
B6
B7
B8
B9

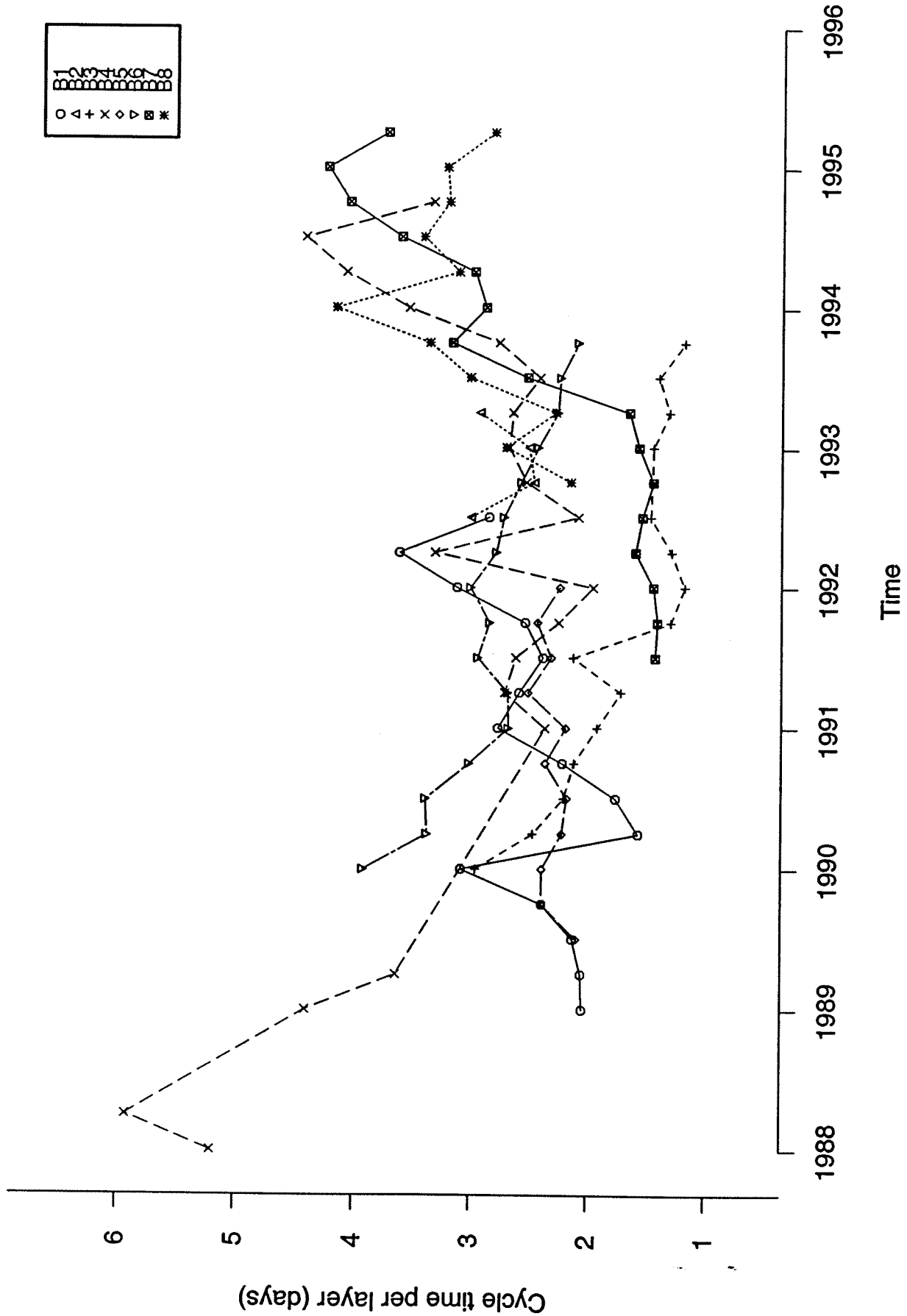


Figure 2.39. MSI Fab Cycle Time Per Layer

Figure 2.40. MSI Fab Direct Labor Productivity

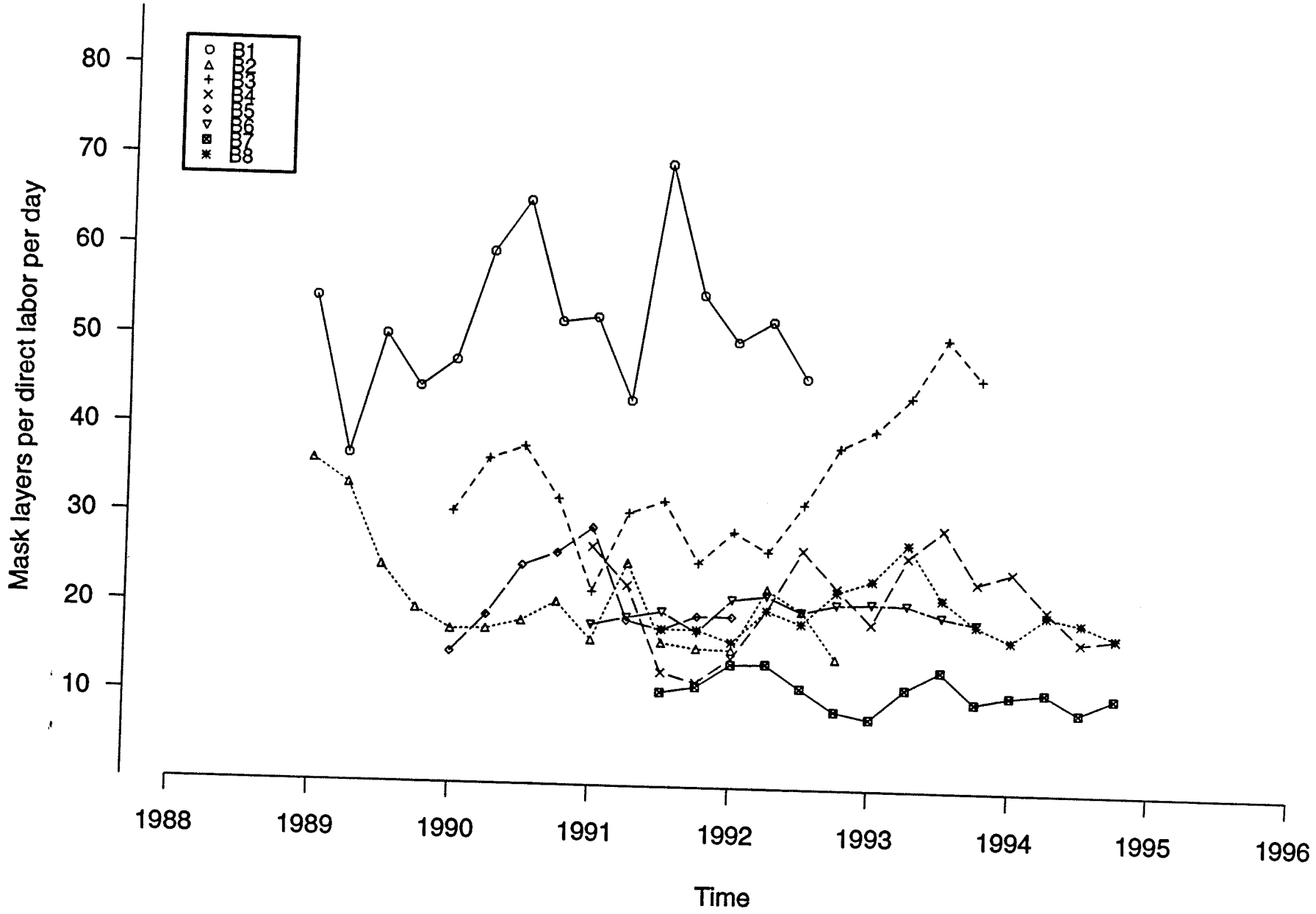


Figure 2.41. MSI Fab Total Labor Productivity

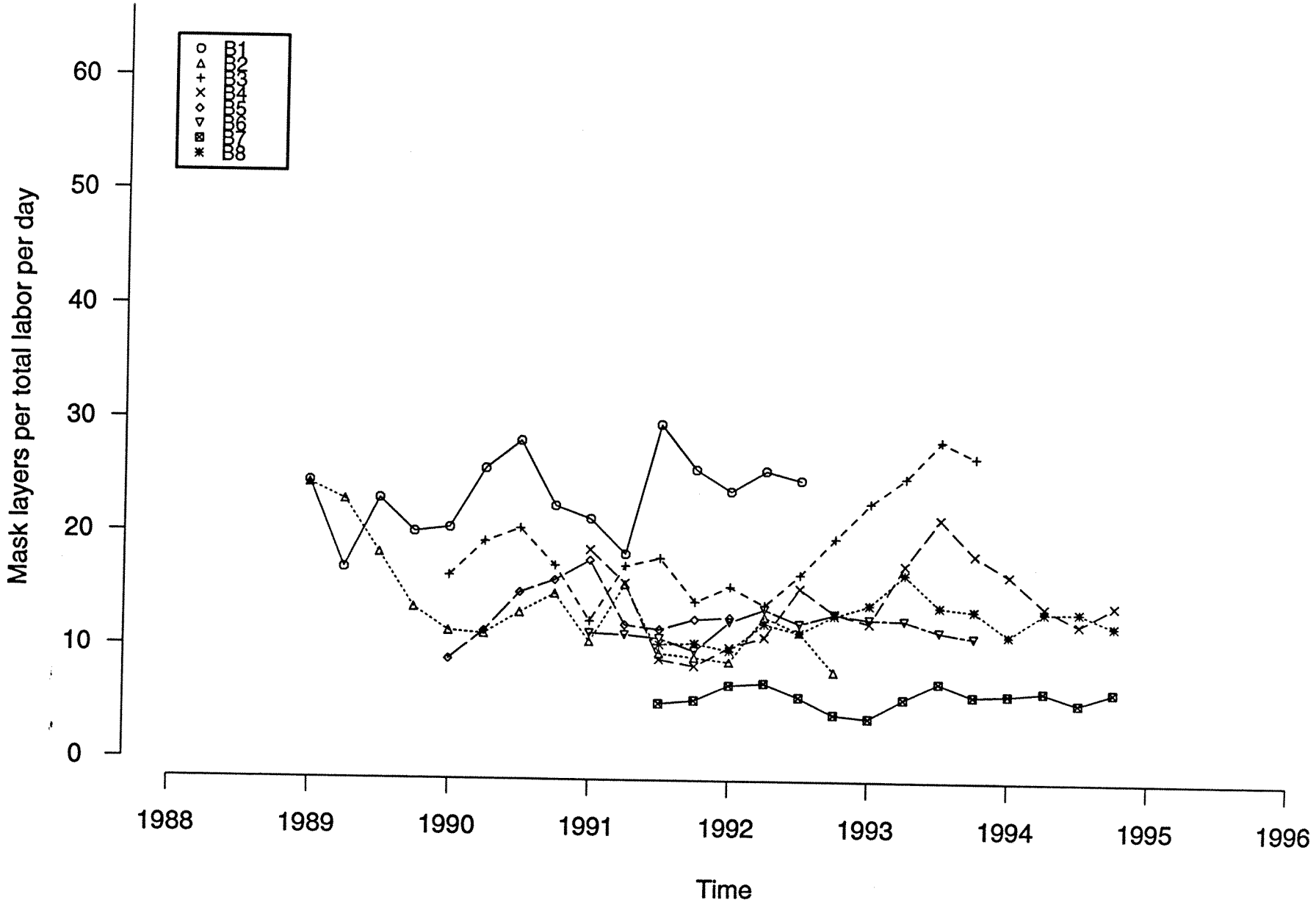


Table 2.32
MSI Fab Line Yields

Fab ID	Time	Line yield per 20 mask layers
B1	3Q92	65.9
B2	2Q93	88.0
B3	4Q93	81.7
B4	4Q94	79.2
B5	1Q92	79.2
B6	**4Q93**	**91.2**
B7	2Q95	67.7
B8	2Q95	68.6

Table 2.33
MSI Fab Defect Densities
1.5 - 4.0 micron CMOS and BiCMOS process flows

Fab ID	Time	Murphy defect density
B1	3Q92	0.94
B2	3Q93	1.68
B4	3Q91	1.49
B5	**1Q92**	**0.89**
B7	2Q95	2.24

Table 2.34
MSI Fab Defect Densities
1.2 - 3.5 micron Bipolar process flows

Fab ID	Time	Murphy defect density
B3	2Q92	3.09
B5	2Q92	0.56
B6	**4Q93**	**0.09**
B7	2Q95	1.46

Table 2.35
MSI Fab Defect Densities
5 - 10 micron Bipolar process flows

Fab ID	Time	Murphy defect density
B1	**3Q92**	**0.79**
B3	2Q92	2.98
B8	2Q95	1.69

Table 2.36
MSI Fab Integrated Yields
1.5 - 4.0 micron CMOS and BiCMOS process flows

Fab ID	Time	Integrated line and die yield (0.5 sq cm die)
B1	3Q92	41.9
B2	2Q93	39.8
B4	4Q93	30.5
B5	**1Q92**	**51.7**
B7	2Q95	28.4

Table 2.37
MSI Fab Integrated Yields
1.2 - 3.5 micron Bipolar process flows

Fab ID	Time	Integrated line and die yield (0.5 sq cm die)
B3	2Q92	20.6
B5	1Q92	55.7
B6	**4Q93**	**88.1**
B7	2Q95	39.5

Table 2.38
MSI Fab Integrated Yields
5 - 10 micron Bipolar process flows

Fab ID	Time	Integrated line and die yield (0.5 sq cm die)
B1	**3Q92**	**45.1**
B3	2Q92	21.5
B8	2Q95	32.1

Table 2.39
MSI Fab 5X Stepper Throughput

Fab ID	Time	Wafer operations per 5X stepper per day
B2	2Q93	231
B3	**4Q93**	**724**

Table 2.40
MSI Fab Ion Implanter Throughput

Fab ID	Time	Wafer operations per implanter per day
B1	3Q92	130
B2	2Q93	201
B3	**4Q93**	**627**
B4	4Q94	160
B5	1Q92	203
B6	4Q93	128
B7	2Q95	137
B8	2Q95	30

Table 2.41
MSI Fab Metallization Machine Throughput

Fab ID	Time	Wafer operations per machine per day
B1	3Q92	31
B2	2Q93	80
B3	**4Q93**	**172**
B4	4Q94	51
B5	1Q92	97
B6	4Q93	48
B7	2Q95	63
B8	2Q95	60

Table 2.42
MSI Fab Cycle Time

Fab ID	Time	Cycle time per mask layer (days)
B1	3Q92	2.9
B2	4Q92	2.5
B3	**4Q93**	**1.2**
B4	4Q94	3.3
B5	1Q92	2.2
B6	4Q93	2.1
B7	2Q95	3.7
B8	2Q95	2.8

Table 2.43
MSI Fab Direct Labor Productivity

Fab ID	Time	Wafer mask layers completed per operator per day
B1	3Q92	46.4
B2	4Q92	15.8
B3	**4Q93**	**46.6**
B4	4Q94	17.3
B5	1Q92	19.4
B6	4Q93	22.3
B7	4Q94	9.9
B8	4Q94	17.9

Table 2.44
MSI Fab Total Labor Productivity

Fab ID	Time	Wafer mask layers completed per person per day
B1	3Q92	24.9
B2	4Q92	8.0
B3	**4Q93**	**27.1**
B4	4Q94	14.1
B5	1Q92	12.8
B6	4Q93	11.1
B7	4Q94	6.3
B8	4Q94	12.2

3. Practices Underlying Performance

In this chapter we report the results of our efforts to correlate the technical performance measurements reviewed in Chapter 2 with managerial, technical and organizational practices of the participants. We present our findings below, organized into sections for the introduction of new process flows, yield improvement, process control, equipment efficiency improvement, cycle time reduction, computer-integrated manufacturing and automation, on-time delivery improvement, and human resources practices.

3.1. Managing New Process Introductions
by Michael Borrus, Nile Hatch and David Mowery

Introduction

For chip-makers, effective management of new process introduction (NPI) can have a decisive impact on the bottom line. Indeed, no area of fabrication practice better illustrates the tight link between manufacturing and market performance in this industry. Effective new process introduction can permit a firm to hit the ground running with timely products at high volumes, thereby maximizing revenues and profits during the characteristic narrow window for reaping price premiums (generally 1-2 years) before intense competition drives prices and profits toward zero.

Conversely, poor management of NPI forces firms to sacrifice significant revenue and profit opportunities when products are relatively late to market with smaller volumes. As in our previous report, [10] we define effective NPI performance as the achievement of relatively low initial defect densities and rapid ramps to relatively high initial wafer start volumes. For the first time, however, we also attempt to evaluate NPI time-to-market -- the opportunity costs (i.e., missed revenues) associated with being late to market in introducing a new process (relative to the earliest entrants). As we will demonstrate later in this section, those costs can be significant and in most cases dwarf the penalties associated with high initial defect densities and slow ramps to volume. In general, it seems it is less costly to be on time with poor yields than to be late with high yields. Of course, as our best performers routinely demonstrate, it is best -- and entirely possible -- to be on time with low initial defect densities and a rapid ramp to high wafer volumes. Indeed, our best performer in sub-micron processes had the lowest initial defect density AND was in production 15 months-to-two years earlier than the rest of our sample.

By "initial defect density" we mean the defect density achieved in the first quarter of production in the volume manufacturing fab after the fab receives the new process from development. We also refer to that initial defect density as the *starting point.* We judge ramps to volume production by comparing first quarter to year-end cumulative volumes in the first year of production. There is no absolute standard -- rather, the best performers define a relative best practice against which the other fabs are compared, qualitatively taking into account, as much as possible,

10. See "Management of New Process Introductions," by M. Borrus, N. Hatch and D. Mowery, in *The Competitive Semiconductor Manufacturing Survey: Second Report on Results of the Main Phase,* R. C. Leachman (ed.), Report CSM-08, Engineering Systems Research Center, University of California at Berkeley, Berkeley, CA 94720 (Sept., 1994).

variations in product mix and firm strategies.

As shown in Table 3.1.1, our most striking finding continues to be the wide disparity in starting points among fabs running roughly similar processes. Starting point variations are especially great in leading-edge processes where the associated penalties for poor performance are also likely to be greatest (because leading-edge processes generally are running the newest products). Starting point variations are less dramatic, though still significant, in older processes.

In general, poor starters improve more rapidly (i.e., they exhibit higher average rates of defect density reduction), perhaps because potential gains from problem solving are greater and easier to come by. However, poor starters typically do not improve fast enough to overtake superior starters in the market relevant time-frame of 1-2 years. Again, this is most evident for leading-edge processes, where there is less convergence of defect densities over time and commensurate greater rewards for getting NPI right.

NPI Strategy

Our data and analysis lead us to an equally striking hypothesis: A firm's strategic approach to product and process design may well be more significant than its routine operational and managerial practices in achieving superior NPI performance and superior NPI time-to-market. In particular, there seems to be great competitive leverage to be gained from adopting a discipline of process design coordination that systematically keeps to a manageable level the amount of change in process steps between new process generations or from one process to another. Such an approach seems especially effective when combined with design (and redesign) for manufacturability practices applied to changed process steps and to the new process product family.

Change-minimizing disciplines work because they exploit accrued knowhow. They ensure that much of an existing 'new' process has already been characterized in the volume production environment and that the knowledge-base and engineering data from the past practice can be applied to ramp the new process. Engineering and technical resources and management attention can be concentrated on solving problems associated with integrating the changed steps or adjusting designs to well-known parameters.

These points are elaborated below. Bear in mind, however, that our work points to the following conclusions without providing sufficient data to statistically confirm them, because the CSM study, with its focus inside the volume fab, was not set up to systematically analyze design approaches outside the fab. We hope, however, to make this issue the subject of an in-depth focus study in future CSM work.

The manufacturing process for semiconductor devices consists of hundreds of operations that are undertaken on a wide variety of processing equipment types. These operations are categorized into broader categories, known as *modules,* that correspond to the particular set of steps used to perform the manufacturing activities in each area of the fab, such as photolithography, etch, implantation, and metallization. The modules currently or previously used in the fab represent its manufacturing know-how and define its technical capabilities. A new process requires three types of process modules: existing modules, new modules using existing equipment, and new modules using new equipment. All of these modules must be integrated to support the new process flow. Although the incorporation of existing modules into the new process

Table 3.1.1.
Performance Measures for New Process Transfers

Fab ID	Initial Defect Density (fatal defects per sq cm)	Average Quarterly Rate of Reduction in Defect Density
Submicron CMOS Processes:		
L1	0.395	-25.4615%
L4	2.919	25.5009%
L5/M5	2.597	30.2656%
L5/M5	1.107	3.9566%
L8	1.010	-1.3923%
L11	0.572	10.5913%
L13	1.290	-3.8180%
L14/M8	4.918	30.0464%
L14/M8	8.412	53.8064%
M1	6.089	59.4945%
M1	0.164	11.8935%
M2/L2	0.614	2.0910%
M3/L9	1.191	9.7213%
M3/L9	0.746	-0.5490%
M3/L9	2.447	14.6494%
M4	0.700	8.0261%
M4	0.377	0.3196%
M6	0.520	18.5136%
M6	0.800	16.1611%
M6	3.090	39.6154%
M7/L12	6.519	18.8139%
M7/L12	3.525	17.0226%
M9	0.769	14.1638%
M10	0.668	2.1271%
M10	0.526	22.7180%
1.0 - 1.2 micron CMOS Processes:		
L2/M2	0.504	3.2236%
L3	1.428	18.2075%
L4	0.645	5.1361%
L5/M5	0.823	2.9346%
L5/M5	1.470	9.5943%
L5/M5	0.828	8.2739%
L6	2.076	2.5960%
L9/M3	0.559	-6.6940%
L9/M3	0.924	-3.8160%
L9/M3	0.739	3.6401%
L10	1.306	11.6606%
L11	1.116	19.3749%

flow appears to be the simplest of the development activities needed for a new process, even this task often encounters unexpected results produced by interactions between existing and new process modules.

Developing and integrating new modules is even more difficult. As a manager from one of the fabs in our study noted, "Every new module will have at least one major problem to solve." In order to develop a new module on existing equipment within a production fab, managers must make tradeoffs between the new modules' needs for experimentation and analysis and the manufacturing requirements of the other production processes.

The most difficult activity in process development is the development of a new module that uses new equipment. In this case, the problems of learning the physical parameters of the process are heightened by the need to learn the peculiar characteristics and parameters of the new equipment.

The challenges associated with developing new modules and incorporating existing modules into new processes are such that careful planning and coordinated development of product and process technology development are essential. For example, if a new process technology is introduced for the manufacture of modifications of existing designs, rather than for an entirely new product design, the introduction of the new process technology is simplified. Indeed, some of the best performers in our study of new process introduction carefully coordinate their introduction of new processes and new product designs as follows: a new manufacturing process is introduced for the production of a shrink of an existing design, rather than being used for the production of a new design. This process is fully characterized and debugged in the manufacturing environment, and then used in the production of the next-generation product design. In other words, the introduction of new products and new processes is staggered, in order to avoid the simultaneous introduction of a new process and an all-new product design into a manufacturing fab. This approach to new process development, however, requires careful coordination of product and process technology development, as well as multi-generational planning of technology development, capacity investment, and equipment procurement.

New processes that incorporate a high percentage of new steps require more time for their development. Shorter development cycles therefore require better planning for the introduction of new products and processes, so that each new process utilizes a substantial share of the steps and modules associated with its predecessor. These advantages can be compounded by design of process, and redesign of product or process, for manufacturability, e.g., the willingness to make mask changes to accommodate manufacturing concerns. While manufacturing organizations can accommodate a remarkable amount of uncertainty and variation in practice, there are clear limits to their operational flexibility. Design practices that either import manufacturing limits from the start or accommodate them later can dramatically ease the NPI task. By relaxing design spec constraints here or designing around production problem areas there, design/redesign for manufacturability is effectively improving the NPI starting point.

Operational NPI Practices

In addition to such strategic considerations, our findings suggest that a range of operational practices can also have a significant impact on superior NPI performance. The addition to our survey of twelve more fabs has resulted in a richer data set that permits substantial refinement of

earlier hypotheses, rejection of some earlier claims and strong verification of others. We will elaborate in more detail later in this section. First, we highlight the significant variations from or confirmations of earlier findings concerning development practices, equipment practices and rates of improvement.

Table 3.1.2 provides data concerning the manpower and time devoted to selected CMOS process transfers at a subset of our participants. Shown in the table are the total times and full-time-equivalent engineers involved in development, hand-off and early-life characterization (i.e., qualification) at the recipient fab, as well as a breakdown of the number of engineers and amount of time from the fab side and from the development side. Also shown in the table are the starting points and the rates of reduction of defect density for these process flows. We subjected these data to a correlation analysis to see if increased manpower or time in development, hand-off, or characterization was associated with improved yields. Basically, we sought negative correlations with initial defect density (i.e., a lower starting point is better) and positive correlations with the rate of reduction (i.e., a higher rate is better).

As Table 3.1.3 shows, we do not find any strong correlations in our small data sample. The most significant beneficial (negative) correlation with NPI starting point is the involvement of fab engineers in process transfer from development to production. It may seem surprising that the number of fab engineers is also negatively correlated with the rate of improvement, as is the time spent by development engineers. We believe this reflects the phenomena that a new process with problems will require engineers to spend more time solving the problems, and firms with NPI problems may have a tendency to throw manpower at the problems. Time spent in development and in hand-off are neutral with respect to initial defect density. Time spent in characterization seems to be counterproductive, again likely reflecting the fact that more problems mean more time is required to solve them.

The keys to success are clearly different from simply devoting an intensive engineering effort to the hand-off from development to production and the qualification of the new process in the production environment. Nor is success simply a function of degree of resources devoted to process characterization in development since our data confirms that there are real limits to how effectively a new process can be characterized for volume production outside of the volume environment. Rather, the intensive involvement of selected experienced volume manufacturing personnel during the late stages of new process development and early-on in the hand-off to the volume fab appears to be a key success factor.

There is some evidence among our best performers that such personnel develop transfer-specific know-how and a kind of specialization in anticipating and solving problems associated with NPI. The enlarged data set strongly confirms our earlier suggestion that what matters most is the continuity and intensity of the development-manufacturing interaction, i.e., the exchange and sharing of the specialized know-how each side brings, rather than the mere formality of assigning fab personnel to development or vice-versa. Indeed, some of our best NPI performers co-locate development activities (e.g. a development fab) and volume manufacturing, while maintaining a clear division of labor and attendant specialization between the two technical workforces. Close spatial proximity facilitates interaction between the two groups and enables development of informal communities of practice between development and fab technical personnel that cut across the formal boundaries of organizational charts and are often the key to solving process

Table 3.1.2 Time and Manpower in Process Transfers vs. Defect Density Performance

Fab ID	Line Width	NPI performance initial DD_o	rate of DD_o improvement	development time	development fte	handoff time	handoff fte	characterization time	characterization fte	process transfer dev engineers num	process transfer dev engineers time	process transfer fab engineers num	process transfer fab engineers time
L4	0.9	2.919	25.5009%	3.0	9.0	1.5	3.0	0.5	0.5	3.0	5.0	4.0	2.0
M4	0.7	0.390	0.3196%	0.0	0.0	2.0	2.0	2.0	3.0	1.0	3.0	1.0	1.0
M4	0.7	0.660	8.0261%	12.0	60.0	3.0	10.0	3.0	6.0	3.0	6.0	3.0	3.0
L5/M5	1.0	0.823	2.9346%	16.0	72.0	1.0	9.5	2.0	19.0	4.0	3.0	6.0	3.0
L5/M5	1.2	0.828	8.2739%	12.0	42.0	1.0	8.0	2.0	16.0	4.0	3.0	4.0	3.0
L5/M5	0.8	2.597	30.2656%	10.0	23.3	1.0	5.0	2.0	20.0	3.0	3.0	2.0	3.0
L5/M5	0.8	1.107	3.9566%	16.0	88.0	1.0	12.5	2.0	25.0	5.0	3.0	8.0	3.0
L3	1.0	1.428	18.0750%	NA	NA	12.0	NA	6.0	NA	0.0	NA	15.0	18.0
L10	1.5	0.638	-0.0911%	24.0	240.0	2.0	4.0	6.0	60.0	3.0	12.0	30.0	12.0
L10	1.0	1.306	11.6606%	2.0	10.0	1.0	3.0	3.0	30.0	4.0	7.0	20.0	6.0
M6	0.6	0.520	18.5136%	24.0	72.0	8.0	32.0	2.0	8.0	2.0	2.0	12.0	6.0
M6	0.7	0.800	16.1611%	18.0	54.0	6.0	24.0	2.0	8.0	2.0	2.0	12.0	6.0
M6	0.5	3.090	39.6154%	60.0	300.0	14.0	28.0	6.0	12.0	2.0	3.0	12.0	6.0
M7/L12	0.8	6.519	18.8139%	6.0	18.0	2.0	4.0	2.0	4.0	1.0	6.0	1.0	2.0
M7/L12	0.8	3.524	17.0226%	24.0	72.0	4.0	16.0	6.0	12.0	2.0	12.0	2.0	4.0
L13	0.9	1.290	-3.8180%	NA	NA	4.0	16.0	8.0	32.0	0.0	NA	2.0	12.0
M4/M8	0.8	4.918	30.0464%	12.0	24.0	2.0	2.0	6.0	6.0	3.0	3.0	1.0	3.0
L14/M8	0.6	8.412	53.8064%	18.0	36.0	6.0	12.0	12.0	24.0	2.0	2.0	1.0	2.0
M9	0.8	0.769	14.1638%	20.0	140.0	4.0	44.0	3.0	6.0	6.0	6.0	20.0	5.0
M10	0.7	0.526	22.7180%	0.0	7.0	NA	NA	3.0	3.0	2.0	4.0	4.0	3.0

rate of DD_o improvement = average quarterly rate of defect density reduction

time = number of months

fte = number of engineering man-months

Table 3.1.3 Correlations Between Transfer Effort and Defect Density Performance

	Development		Handoff		Characterization		Process Transfer			
							Dev Engineers		Fab Engineers	
	time	fte	time	fte	time	fte	number	time	number	time
Initial Defect Density	0.078	-0.139	0.073	-0.222	0.527	-0.101	-0.147	-0.052	-0.414	-0.285
Quarterly Rate of Reduction in Defect Density	0.301	0.011	0.425	0.111	0.402	-0.287	0.041	-0.333	-0.237	-0.244

Abbreviations: fte - number of full time equivalent engineers

problems.

For commodity product NPI, appropriate use of a development fab running pilot production volumes in the new process is an essential key to superior performance. In general, the development fab provides a pre-volume process characterization, early production problem identification, substantial reference data, and partially processed wafers for comparative engineering tests. These beneficial impacts were magnified where equipment sets could be exactly duplicated between the development and volume fabs. Indeed, the very best performers either ran their development fab with substantial matching equipment in parallel with the production fab in the early stages of qualification or, in one case, routinely builds a new development facility which is expanded into the volume facility with each new process generation, thereby maintaining exact equipment duplication. Of course, the extraordinary expense of the latter strategy is simply unavailable to most firms, and equipment duplication is increasingly hard to manage as a fab ages or runs multiple processes over time. Indeed, reflecting the particular characteristics of their multi-process, multi-product flow business, most ASIC firms used no development fab at all. The ASIC superior NPI performers instead relied to a much greater extent than most commodity firms on the strategic design approaches elaborated above and on developing rigorous NPI routines and a workforce with NPI specialization. In essence, for those firms, NPI becomes the kind of focused religion that TQM yield management or total asset productivity becomes for the best performers in those respective domains.

Modeling the Determinants and Effects of Successful New Process Introduction

Our field research has led us to distinguish at least three general approaches to managing new process introduction. In our sample, one group of fabs introduces new processes that are well-understood, exhibiting relatively low defect densities at their inception. A second group of fabs introduces new processes that are less well-characterized, and attempts to improve their performance through learning by doing in the manufacturing fab. A third group of fabs focuses on the incremental development and modification of manufacturing processes, frequently introducing new processes and constraining the development of new products to conform to the constraints imposed by the development of their manufacturing process technologies. This last group of fabs consists mainly of producers of ASICs that operate as foundries.

Data were collected (Table 3.1.2) for selected CMOS process transfers at a subset of the fabs concerning the length of time and the number of engineering-months involved in the following stages of new process introduction: (1) development of the process; (2) the hand-off from the development to the production phases; and (3) the qualification ("characterization") of the new process in the volume manufacturing facility. These data cover a growing number of our sample of fabs, and weakly reveal several patterns.

Correlation results are displayed in Table 3.1.3. The length of time required for new process development does not appear to support superior performance (insofar as this is measured primarily by initial defect density). Indeed, lengthy development time can imply a process with minimal overlap to predecessors which will require lengthy characterization in the production environment. However, as suggested earlier, there are weak correlations between superior NPI performance and engineering-effort devoted to process transfer, especially by volume fab technical personnel. Not surprisingly, fabs that invested time in hand-off and process characterization

also tended to show more rapid rates of yield improvement during the first year of production.

The uncertainties of many aspects of semiconductor manufacturing mean that most non-ASIC producers employ a dedicated development facility for new process development. Debugging a new process in a development fab is more effective when the development fab resembles the manufacturing fab in as many aspects as possible, particularly in the equipment and materials used. Reflecting the complexity of semiconductor manufacturing, as well as the frequent need to alter production equipment as part of new process introduction, differences between the development facility and the manufacturing fab in their equipment sets and configurations can impede new process introduction. In response to this, a number of the fabs in our sample have adopted policies that require that the receiving fab have an equipment set that is identical to that on which a new process is developed in the development facility.

Even stringent requirements for equipment duplication, however, cannot eliminate all significant differences between the manufacturing environment and that of the development fab for some products or processes. In the case of DRAM products, the differences in manufacturing volumes between the development and manufacturing facilities of leading producers are so great that development fabs cannot fully replicate manufacturing conditions. This factor has contributed to the efforts of some DRAM manufacturers to move new processes out of their development fabs and into manufacturing more rapidly and at lower levels of process characterization.

Table 3.1.1 reveals substantial performance differences among manufacturing facilities in the CSM database (a group that includes producers of DRAMs and other memory products, logic, and ASIC products), measured as either the initial defect density for a new manufacturing process (the defect density reported for the first quarter of operation of a process in the manufacturing facility) or the average quarterly rate of improvement of defect density.

The penalties associated with a poor start, i.e., a high initial defect density, are often very difficult to overcome. Figures 3.1.1 - 3.1.2 graph defect densities on normalized scales vs. time for our participants in submicron and 1.0-1.2 micron categories, respectively. These data reveal that fabs that began with very high defect densities in new manufacturing processes found it very difficult to close the gap with the facilities that began with much lower defect densities.

Manufacturing processes that are closer to the technological frontier, which in this case are associated with smaller linewidths on semiconductor chips, display an even more pronounced poor-start penalty. The data in Figures 3.1.1 - 3.1.2 suggest that firms that begin with poor defect densities in submicron linewidth semiconductor manufacturing processes find it much harder to close the performance gap with the leaders. This result, of course, is precisely what one would expect -- labor turnover, technical journals, and other sources of inter-firm spill-overs take time to transmit knowhow among competitors, and a superior starting point in the most advanced manufacturing processes therefore yields more enduring competitive advantages.

Statistical analysis of new process introduction revealed several interesting findings. The rate of improvement or learning associated with a new manufacturing process was not solely determined by expansion in volume, but could be increased by allocating more engineering resources to the experiments and organized problem-solving activities that are necessary to reduce parametric defect densities. These results suggest that in semiconductor manufacturing, learning by doing is not exogenous, but can be increased by management decisions. The

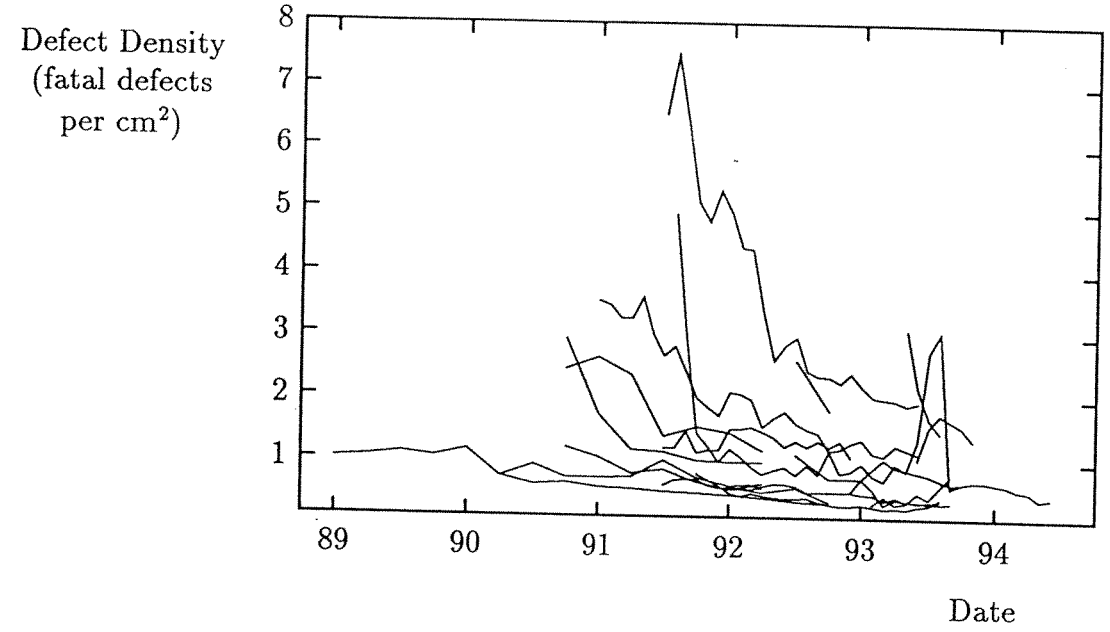


Figure 3.1.1
Defect Densities of Submicron CMOS Process Flows

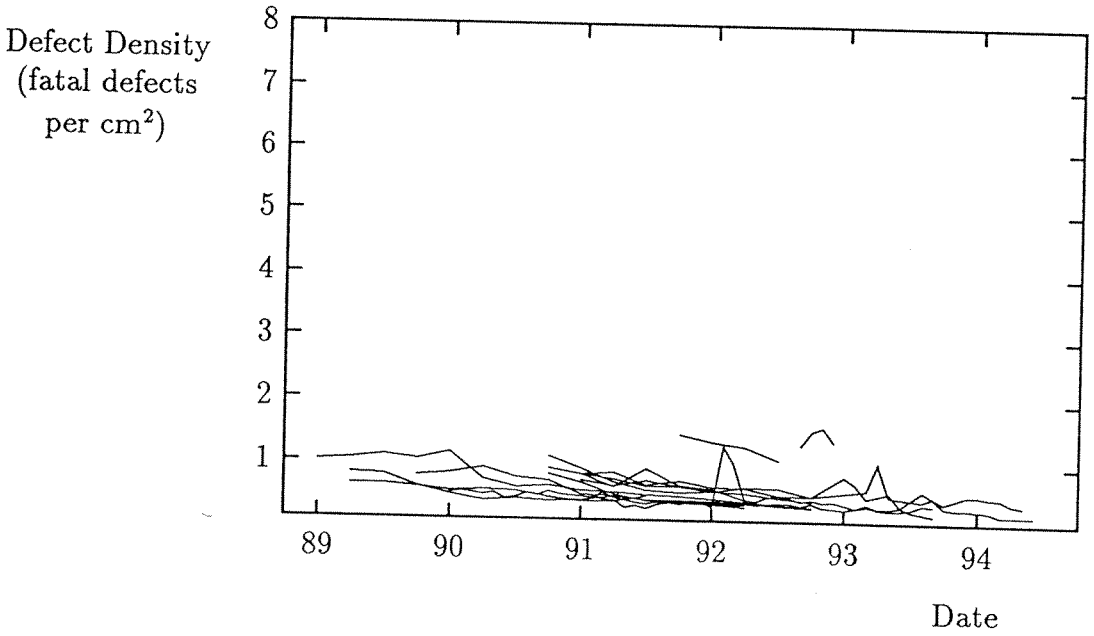


Figure 3.1.2
Defect Densities of 1.0-1.2 micron CMOS Process Flows

allocation of engineering resources to problem-solving activities for a new process, however, affects the rate of improvement in other manufacturing processes being operated in the same facility.

Since most new semiconductor manufacturing processes are introduced into facilities that are simultaneously operating other, more mature processes, a poorly managed new process introduction can have broader effects on a firm's competitive performance. Yields and output of both a new product and existing products manufactured with more mature processes may all be reduced by an unsuccessful new process introduction. The negative effects of a new process introduction on manufacturing performance for existing products thus may increase the costs associated with the introduction of a poorly characterized manufacturing process into a commercial-volume fab. These costs reduce the profits associated with a first-to-market strategy that relies on extensive characterization of a new manufacturing process in a production fab that is operating older manufacturing processes. [11]

The analysis of management techniques for new process introduction also yielded some interesting results. The use of a dedicated development fab was associated with superior performance in improving defect densities, and locating this development facility on the same site as the high-volume manufacturing facility that was to receive the new process improved performance. Finally, identical production equipment in the development and manufacturing facilities was associated with better performance. Our model also suggests that there are important differences among product classes in the management and learning behavior associated with new process technologies. As we noted earlier, ASIC producers are more likely to introduce incremental modifications of their process technologies much more frequently, and are less likely to utilize development facilities. The management variables that were important in explaining interfirm differences for our broader sample were much less powerful for this product class. In DRAM manufacturing, we find that most of the critical problem-solving and learning associated with new manufacturing processes takes place in the first generation of a new family of DRAMs, e.g., the first product design and associated process for a 4MB DRAM. Later shrinks of that DRAM product experience fewer problems in process development and transfer.

Although the statistical analysis revealed some generic practices that contributed to superior performance, firm-specific effects remained significant, as a fixed-effects model showed. These statistical results are consistent with a view of new process introduction that emphasizes interfirm differences in performance, especially in the most advanced products, and that stresses the role of management techniques in improving or degrading the smoothness of the transfer and the rate of learning. Semi-scale development facilities improve firms performance in products other than ASICs, while significant differences among product classes affect firms new process introduction. But considerable firm-specific variance remains unexplained, and requires a more detailed examination.

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11. The negative effects of new process introduction on existing processes will be higher still when more than one new manufacturing process is introduced simultaneously, something that was attempted in several of the fabs in our study.

Measuring the Costs of Poor Performance in New Process Introduction

To further illustrate the importance of introducing a new process technology early and with high yields, we simulate the penalties associated with a poor start using the data from CSM study. The losses associated with late start are largely opportunity costs. They include not only lost revenues from the periods before the process is introduced, but also the revenue premiums that are foregone because prices are falling.

In contrast, the penalties associated with poor starting yields are primarily additional manufacturing costs generated by producing non-functioning chips. Figure 3.1.3 shows the price trends of four recent generations of DRAM products. The precipitous decline in prices observed here is not restricted to memory products, but applies to most semiconductor products. Early innovators enjoy a substantial price premium while supply remains relatively limited. As more firms enter the market, however, and as fabs reduce costs through learning by doing, production expands and prices fall rapidly. Entering the market later than competitor firms imposes large penalties in the form of lost revenues.

To see this effect in more detail, consider the case of 4 MB DRAM products. Figure 3.1.4 shows the price path for this product through time, along with the dates at which eight new 4 MB DRAM manufacturing processes were introduced into manufacturing. Our small sample does not include the earliest innovators in this product market and therefore excludes the first-movers that obtained very large price premiums in 1989. We can estimate the penalty a firm incurs through late entry, however, by calculating the difference between the prices they would have obtained each period had they been first to introduce the process, versus the prices obtained when they actually entered. For example, the penalty of delay in the first period after a new process is introduced is the difference between the price of the product in 1989, when the 4MB DRAM was first reached the market, and the price obtained by a later entrant in its first period of production. The penalty of delay in the second period of production is the price of the product in its second period in the market less the price the firm receives in its second period of production, and so on. In Table 3.1.4, we present estimates of both the monthly price penalties associated with delayed entry for each of the 4 MB DRAM processes in our sample and estimates of the penalty from poor yields that are described below.

The high costs of delayed entry into a new product market mean that firms face significant incentives to be first to market with new products at almost any cost. But early entry has its costs, which may offset the higher unit revenues for good die that are associated with early entry. The most obvious reason to postpone entry is the need for additional time to develop and debug a product design or the new process sufficiently for volume manufacturing. [12] Firms have considerable discretion in the degree to which they characterize a new process in development before transferring it to a high-volume manufacturing environment. When an poorly characterized process is transferred to the manufacturing facility, [13] it will typically suffer serious yield problems, imposing the penalty of added costs due to the poor starting yields of the new process.

12. Our data suggest that the process development problems dominate product design problems in causing these entry delays.

13. Differences between the development and manufacturing environments can often create a need for further development work in the manufacturing facility, especially for products such as DRAMS, that are produced in high volumes. Some of the firms in our study stated that they now try to release new processes into their

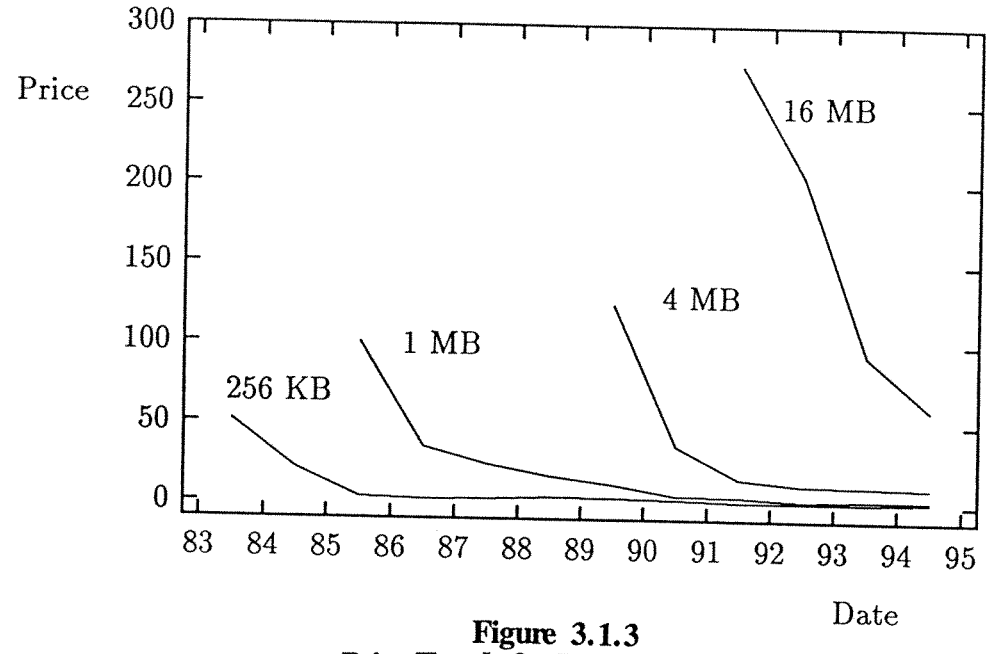

Figure 3.1.3
Price Trends for DRAM Products

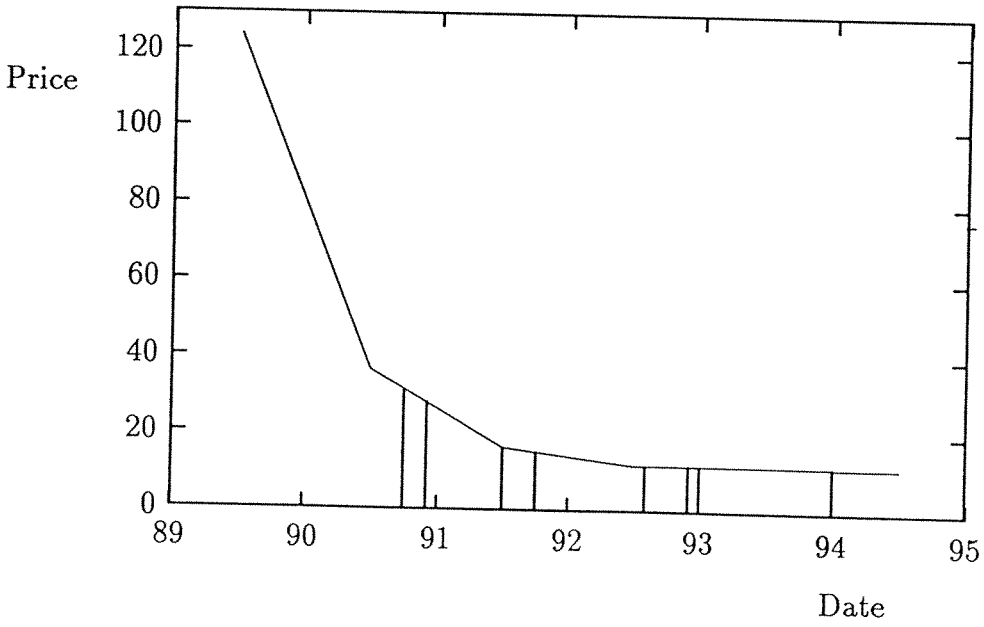

Figure 3.1.4
Price Trend and Start Dates for 4 MB DRAM Products

Table 3.1.4
Monthly Penalties Per Unit Associated with Late Start and With Poor Yields for a Sample of 4 MB DRAM Processes

Process 1		Process 2		Process 3		Process 4		Process 5		Process 6		Process 7		Process 8	
Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield	Delay	Yield
$92.59	$0.00	$95.94	$0.00	$107.65	$6.12	$108.71	$6.71	$111.89	$680.29	$111.93	$2.18	$111.94	$0.06	$112.16	$0.51
86.97	0.00	90.31	0.00	100.71	6.35	101.76	5.21	104.60	1465.63	104.64	5.59	104.65	1.31	104.89	0.74
81.34	13.56	84.69	0.00	93.76	12.34	94.82	5.30	97.31	478.34	97.35	2.63	97.36	1.40	97.62	0.64
75.72	10.33	79.06	0.00	86.82	5.16	87.87	0.41	90.02	94.46	90.06	0.00	90.07	1.47	90.35	0.98
70.09	10.11	73.44	0.00	79.87	3.43	80.93	0.78	82.74	46.14	82.77	1.10	82.78	1.92	83.08	0.00
64.47	7.52	67.82	0.00	72.93	4.42	73.98	1.35	75.45	18.60	75.48	1.32	75.49	3.70	75.81	0.00
58.85	4.46	62.19	0.00	65.98	2.48	67.04	0.82	68.16	8.91	68.20	1.90	68.21	3.29	68.54	0.00
53.22	5.78	56.57	0.00	59.03	5.01	60.09	0.43	60.87	27.76	60.91	1.88	60.93	3.51	61.26	0.00
47.60	7.07	49.62	0.00	52.09	5.95	53.15	0.00	53.58	50.81	53.64	2.37	53.66	3.48	53.99	0.00
41.97	8.61	42.68	0.00	45.15	5.53	46.20	0.00	46.29	6.61	46.37	1.70	46.40	4.67	46.73	0.00
35.03	5.95	35.73	0.00	38.20	8.72	38.91	0.00	39.01	0.00	39.10	1.92	39.13	3.15	39.46	0.12
28.08	6.07	28.79	0.00	31.26	7.09	31.63	0.00	31.72	0.00	31.83	0.00	31.86	3.55	32.19	0.03
21.14	4.31	21.84	0.00	24.31	7.23	24.34	0.00	24.45	0.00	24.56	0.65	24.59	3.92		
19.82	5.18	20.52	0.00	22.65	5.15	22.67	0.00	22.80	0.00	22.91	1.38	22.94	4.08		
18.50	4.85	19.20	0.00	20.98	4.32	21.01	0.00	21.16	0.00	21.27	1.40	21.29	2.97		
17.18	4.10	17.88	0.00	19.32	9.83	19.35	0.00	19.51	0.29	19.62	0.83	19.65	3.71		
15.85	4.87	16.56	0.00	17.65	5.14	17.68	0.00	17.86	0.00	17.97	1.39	18.00	2.90		
14.53	4.61	15.24	0.00	15.99	4.83	16.02	0.09	16.22	0.00	16.33	0.52	16.36	2.87		
13.21	4.16	13.92	0.25	14.33	3.05	14.35	0.00	14.57	0.00	14.68	0.82	14.71	2.72		
		12.60	0.36	12.66	5.09	12.69	0.00	12.93	0.00	13.04	0.60	13.06	2.34		
		10.93	0.02	11.00	3.27	11.02	2.43	11.28	0.00	11.39	0.48	11.42	2.85		
		9.27	0.44	9.33	4.43	9.36	2.40			9.74	0.20	9.77	2.69		
		7.60	1.81	7.67	5.43	7.71	4.37			8.10	0.19	8.13	2.71		
		5.94	1.40	6.00	4.27					6.45	0.00				
		4.28	1.09	4.34	4.44					4.81	0.00				
				4.01	4.85										
				3.69	4.27										

Although flawless introduction of a new product results in high yields and revenues, in practice, early transfer of the manufacturing process often exacerbates yield problems. To illustrate the penalty associated with poor starting yields, we present another simulation, again based on the sample of 4 MB DRAM processes from the CSM survey. We base this simulation on the assumption that the cost of manufacturing a wafer is basically constant. Therefore, the cost of producing an individual chip, whether it functions or not, depends on the wafer size and the die size. Let the wafer size be A sq cm and let the die size be a sq cm. Then the gross number of dice on the wafer x is A/a. [14] If we denote the manufacturing cost of a wafer as W, then the unit cost per die is

$$w = \frac{W}{x} = \frac{W * a}{A}.$$

Now we introduce the influence of yield losses on manufacturing cost. If we let $y(t)$ denote the manufacturing yield at time t and q denote the number of functional dice produced, then $x * y(t) \equiv q$, by definition. [15] Since the good output must bear the cost of yield losses, the manufacturing cost can be represented as $w * x = c * q$, where c is the average variable cost of good output. Thus, the unit cost of production, including the cost of yield losses, is

$$c = w/y(t).$$

Using our sample of new 4 MB DRAM processes, we simulate the cost penalties associated with the actual yields obtained after the processes are introduced into the manufacturing environment. This requires the simplifying assumption that all the processes have a manufacturing cost of $1000 per eight
inch equivalent wafer. [16] Using actual process yield data and the assumed wafer cost, we simulate the cost penalty associated with poor starting yields. This penalty is defined as the additional cost incurred by a producer whose yields are below those of the best of our eight DRAM producers each period. These penalties are computed only for the processes in our sample. [17] The results of our simulations are presented in Figure 3.1.5. [18]

Figure 3.1.5 shows that the differences in yield and the resulting cost penalties are quite volatile and occasionally large. The average cost of a die, ignoring yield losses, is $15. Thus, the yield penalty of almost $14 faced by one of the early processes effectively doubles the manufacturing cost relative to the process with the best yields. These results show that the penalty for poor yields often is substantial in the early operation of a new process, and the variation among

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production facilities at lower levels of characterization because of concerns over being late to market.

14. For our purposes, we ignore the lost silicon at the edges of the wafer.

15. We assume that yield is a function of time to allow for yield improvements. In fact, yield is not solely a function of time; its improvement depends on product and process design, process development and transfer characteristics, and manufacturing practices.

16. This assumed wafer cost is consistent with the estimated wafer costs corroborated by the firms participating in the CSM survey.

17. There were many other 4 MB DRAM processes in production during this period that are not in our sample, some of which potentially had higher yields than any in our sample.

18. One of the processes in the sample began with extraordinarily low yields, resulting in a cost differential as high as $1465.63 per unit. To better illustrate the cost variation in most of the processes, the scale of the figure is chosen such that the early cost penalties of this unusual process are not visible.

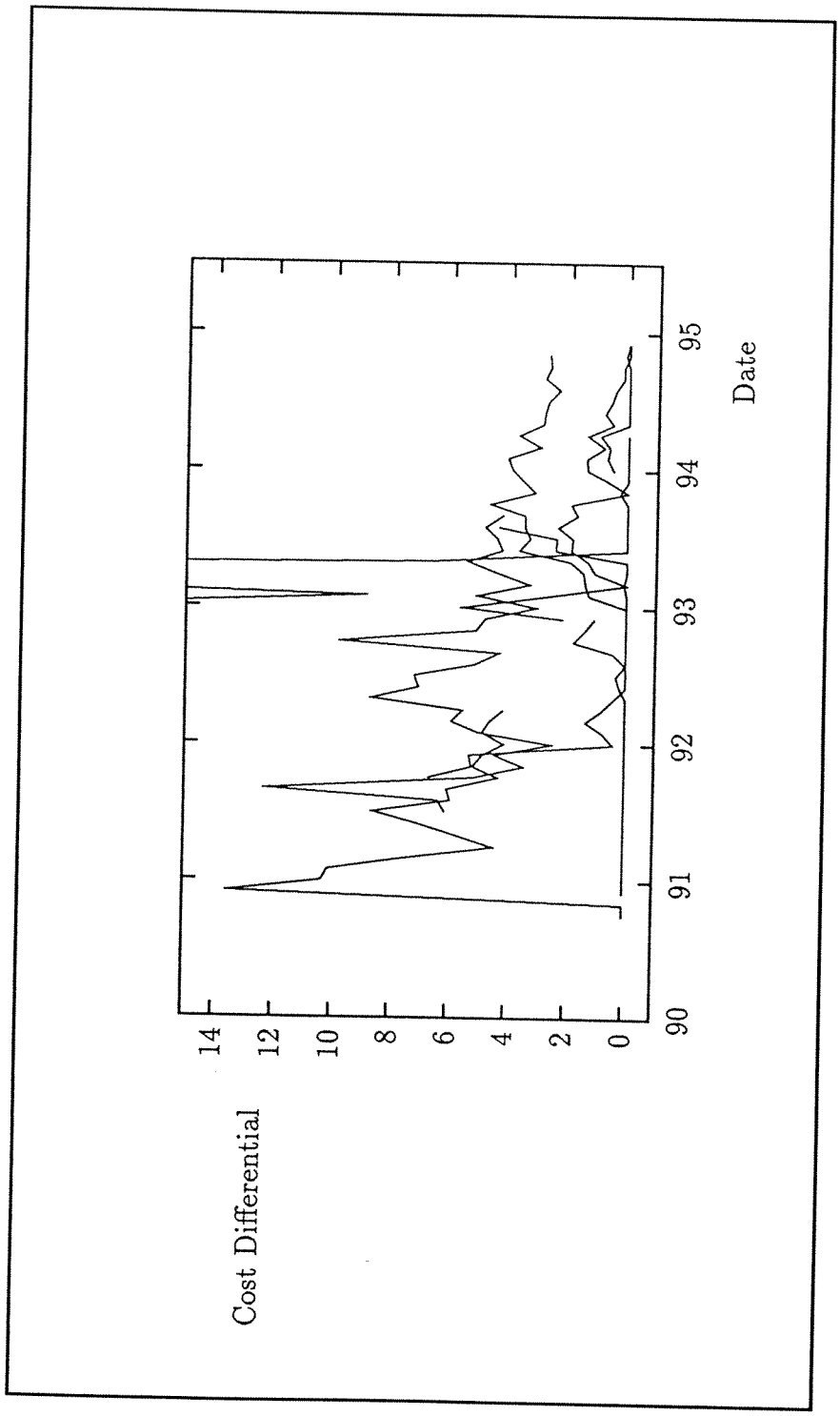


Figure 3.1.5
Simulated Penalties for Poor Yields Among New 4 MB DRAM Processes

firms in cost differentials is largest early in the life of the process. The costs of different producers appear to converge somewhat over time, although even after three years the differences persist. Comparison of the two columns for each manufacturing process in Table 3.1.4 makes it clear that the penalties associated with late entry dominate those associated with poor starting yields. Time to market is critical to competitive advantage in DRAMs. Nonetheless, the penalties associated with poor starting yields are considerable.

3.2. Yield Improvement
by George McMurray

This section updates previous work concerning die yield and provides new analysis in the area of line yield. The first-time reader is referred to the previous edition of this section (Cunningham et al [1994] [19]) for a review of yield modeling. First, we analyze the line yield rate across the fabs studied. Second, we present a regression model which attempts to explain die yield. The most significant addition to the analysis of yield since the last report is that of product type. Three product categories are established: Memory, Logic and Medium Scale Integration (MSI) products. The Memory fabs in our survey produced products ranging over 4-16M DRAMs, 256K, 1M and 4M SRAMs, EEPROMS, and ROMs. Logic fabs produced Microprocessors, Gate Arrays and other ASIC products. The MSI fabs are typically older fabs (10 or more years) and produced lower device-count products such as TTL logic and Analog circuits. The MSI fabs used Bipolar technology, BiCMOS and CMOS (1.5 micron or larger). The memory fabs used CMOS and usually had the smallest feature sizes. The logic fabs also used exclusively CMOS but tended to lag memories in feature size.

Line Yield

Line yield *LY* deals with the wafer losses prior to die electrical test. Line yield responsibility is typically assumed by manufacturing or process engineers. The line yield data is normalized by the number of mask layers to take into account the varying complexity of the processes. Typical losses due to line yield are misprocessing or mishandling which result in the scrapping of whole wafers or entire lots of wafers. Cunningham et al [1994] mention two factors as to why reported line yields might be inflated:

1. Poor prediction capabilities of die yield from in-line inspections leads to a policy of continuing to process marginal wafers through to die sort in order to see what happens.

2. Line yield has historically been one of the metrics for wafer fab productivity and so there has been an incentive to pass on marginal wafers to die sort. As die sort responsibility has historically been held by other organizations (e.g. Product Engineering), this has led to suboptimization (i.e., myopic behavior).

Later in this section we examine a regression model which attempts to explain line yield. In Section 3.3 (Process Control), we examine the trends of line yield.

Analysis of Line Yield

The analysis of line yield incorporates a regression model which attempts to explain line yield as a function of process age, the fab type (i.e. Memory, Logic or MSI) and whether or not recipe download was automated or not. We found numerous fabs had implemented automated recipe download to reduce the number of errors from misprocessing. The logarithm of process age in months was used in the model for reasons similar to that stated in previous work

19. See "Yield Improvement: Results and Best Practices," by Sean Cunningham, Costas Spanos and Katalin Voros, in *The Competitive Semiconductor Manufacturing Survey: Second Report on Results of the Main Phase,* R. C. Leachman (ed.), Report CSM-08, Engineering Systems Research Center, University of California at Berkeley, Berkeley, CA (Sept, 1994).

(Cunningham et al [1994]). The data used in this analysis comes from the last two quarters of reported line yields, so that the most recent manufacturing practices could be evaluated. Table 3.2.1 presents the various factors examined in the linear model as potential explanatory variables for line yield.

Our statistical analysis resulted in the following model significant to 5%. Other variables (process age, number of clean rooms, number of subprocesses, number of active die) were not well-correlated with performance.

$$LY = a_0 + a_1 * Type + a_2 * Autorec \ .$$

Further analysis showed that *Autorec* and *Type* were co-linear, so the *Autorec* was dropped as a factor since *Type* seemed to be a better explanatory variable. The resulting values of the coefficients along with the standard errors are as follows:

$$a_0 = 99.91 \ \ (+/-4.79), \ \ a_1 = -7.43 \ \ (+/-2.19)$$

The regression yielded an R^2 value of only 0.45, indicating that the model could not explain the majority of the variation in line yields.

The memory fabs in our survey tend to have more recent equipment and automation, including automated recipe download. Of the ten memory fabs, two had 100% automated recipe download, and all but two had partial applications. These two memory fabs didn't seem to suffer in line yield as they still achieved high line yields, perhaps reflecting their narrow process and product focus. In contrast, most of the MSI fabs were built over 10 years ago, prior to automated recipe download capabilities. As a result only one of the eight MSI fabs had gone back and installed auto recipe download. The MSI fab with auto recipe download was third out of six in line yield performance. The logic fabs were split into two groups, with 7 having installed a significant amount of automated recipe download and 9 not having done so. It is clear from the boxplot in Figure 3.2.1 that the logic fabs with auto recipe download had higher line yields than logic fabs without auto recipe.

Die Yield

Die Yield *DY* represents the fraction of die from each wafer which pass electrical multiprobe test and visual inspection. Some of the causes for failure at multiprobe include defects, parametric shifts in the process, and test related issues. In general, management of die yield is more complicated than line yield, as each die has a different level sensitivity to defects and parametric shifts due to design and customer requirements. It is useful to partition of *DY* into a random component which is generally regarded as defect related (*YDefect*) and a clustered component (*YCluster*). Often *YDefect* is modeled as a Poisson random variable while *YCluster* is estimated using a clustering algorithm. In an attempt to compare die yields across the industry, we have used a Murphy model which relates yield to defect density and die area by the following equation:

Table 3.2.1. Values of Explanatory Variables for Line Yield Performance

Fab ID	Tech	Type	ProcAge	CleanRm	SubProc	ActiveDie	Autorec
M1	CMOS	Mem	12	3	1	6	1
M2/L2	CMOS	Mem	27	17	4	400	1
M3/L9	CMOS	Mem	63	4	55	320	1
M4	CMOS	Mem	22	6	5	12	1
M5/L5	CMOS	Logic	24	3	3	40	0
M6	CMOS	Mem	5	5	3	15	1
M7/L12	CMOS	Logic	30	3	9	85	1
M8/L14	CMOS	Mem	13	1	3	40	0
M9	CMOS	Mem	30	3	2	3	0
M10	CMOS	Mem	37	1	7	10	0
L1	CMOS	Logic	9	2	5	85	1
L3	CMOS	Logic	17	3	1	13	0
L4	CMOS	Logic	28	1	4	50	1
L6	CMOS	Logic	52	1	12	200	1
L8	CMOS	Logic	72	1	1	5	1
L10	CMOS	Logic	18	1	2	10	0
L11	CMOS	Logic	33	15	7	600	0
L13	CMOS	Logic	31	2	5	150	1
L15	CMOS	Logic	12	1	3	15	1
L16	CMOS	Logic	14	3	3	50	1
B1	CMOS	MSI	48	1	3	65	0
B2/L7	Bipolar	MSI	14	2	10	400	0
B3	Bipolar	MSI	48	2	6	180	1
B4	CMOS	MSI	76	1	4	61	0
B5	Bipolar	MSI	33	1	3	45	0
B6	Bipolar	MSI	48	2	10	212	0
B7	Bipolar	MSI	48	1	5	200	0
B8	Bipolar	MSI	14	1	5	130	0

Abbreviations: *Yield* is the line yield per 20 layers (i.e., line yield normalized by the number of mask layers. *Tech* is the process technology type. *Type* is the fab type. *ProcAge* is the process age in months which is used in the model analysis. *CleanRm* is the number of clean rooms in the fab. *SubProc* is the number of different subprocess options run in the fab (e.g. single vs. double layer metal). *ActiveDie* is the number of active die which are run in the fab. *Autorec* is an indicator variable for the presence of automated recipe download capability, with a value equal to 1 indicating its presence. *NA* indicates data not available.

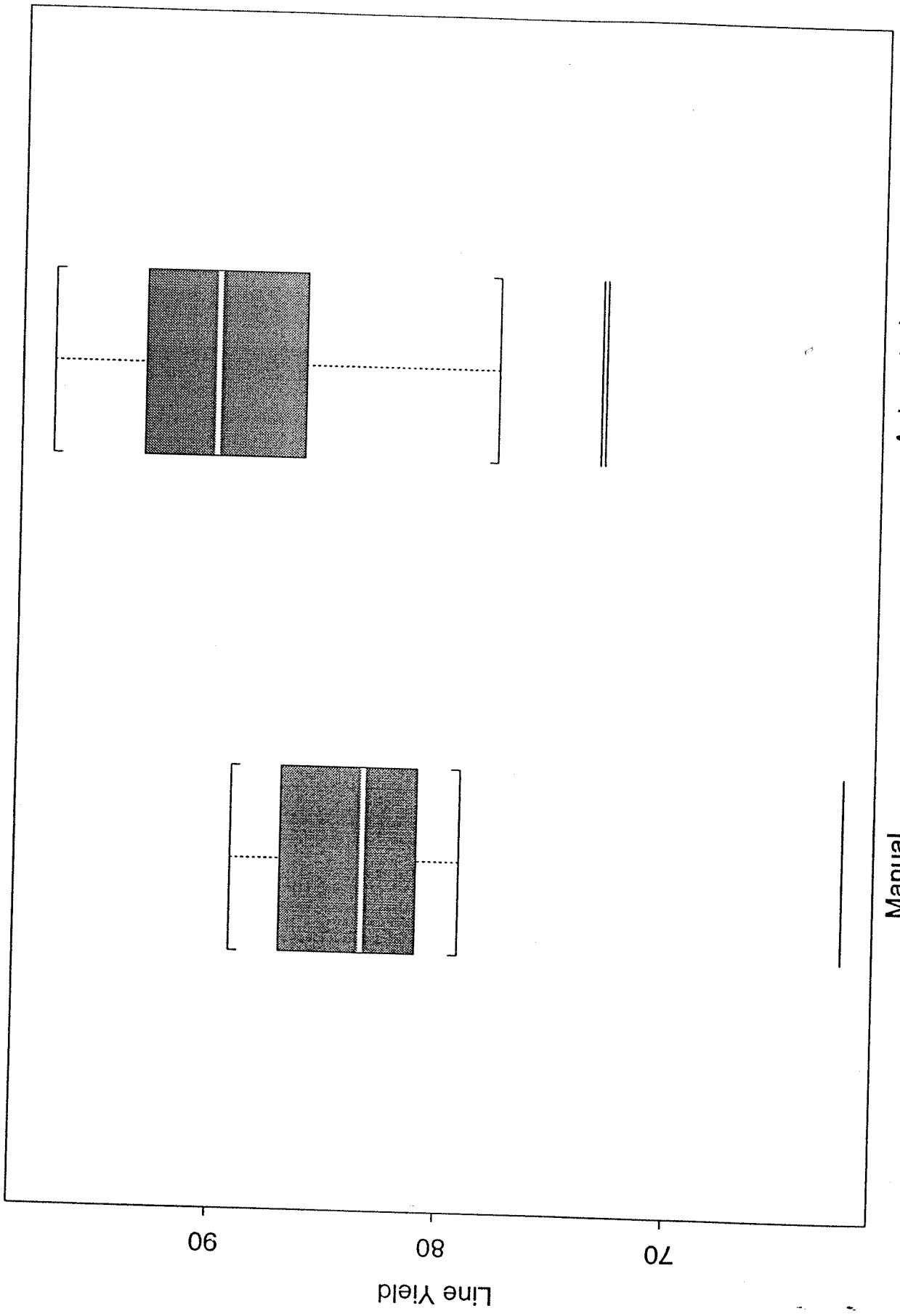


Figure 3.2.1
Boxplot of Line Yields for Logic Fabs:
Automated Recipe Load vs. Manual Recipe Load

$$DY = \left[\frac{(1 - e^{-AD})}{AD} \right]^2$$

where A is the die area in sq cm and D is the average number of fatal defects per sq cm.

A wide range of yield models have been used in the industry. A good survey can be found in Cunningham [1990] [20]. Particles and crystal defects are examples of defects which can cause die to malfunction. Advanced logic and memory devices tend to have defect limited yield. Memory die are unusual in that a high percentage of the die area is circuitry with critical spacing, making them particularly vulnerable to defects. To compensate for this vulnerability, substantial redundant circuitry is incorporated in memory devices to improve die yield.

Die yield also can be partitioned into the following two groups depending on the severity of the failure: Functional and Parametric. A functional failure does not operate even at the simplest level (e.g., output doesn't switch from high to low). Die which suffer parametric failures still operate but not within specifications (e.g., lower frequency, slower speed, input voltage threshold out of range). Tight die product performance specifications can limit the functional yield as well. In Analog die, the degree of component matching dictates the level of die yield. Component matching can be upset by slight parametric process shifts.

In general, the memory and logic fabs all have defect limited die yields and hence have focused there yield efforts on particle elimination. On the other hand, the MSI fabs which build die to larger design spacing (e.g. metal pitch > 1.5 micron) are less sensitive to particle defects and have die yield which is limited by parametric issues. It is difficult to compare die yields across the fab types mentioned above since there doesn't exist a yield model we can calibrate from the survey data which effectively handles all issues mentioned.

The remainder of this section develops a linear statistical model which regresses die yield rate against various technological product-related and facility-related factors.

Die Yield Analysis

There are two candidate metrics which we examined for our linear model: defect density, and W, which is a transform of the die yield defined as follows.

$$W = \log [DY/(1-DY)] .$$

W has the appealing property that, as DY approaches one, the derivative with respect to any particular regressor variable is decreasing, i.e., it will reflect the characteristic that it is more difficult to achieve large gains in yield with a high-yielding process than with a low-yielding process.

Defect density is also a transform of the reported yield and die area. As mentioned earlier, the Murphy model was used to estimate defect density. In Figures 3.2.2 - 3.2.4, we present some box plots of die yield, defect density and W for the three fab product types.

20. Cunningham, J. A., "The Use and Evaluation of Yield Models in Integrated Circuit Manufacturing," *IEEE Trans. Semicond. Manufact.* **3** (2), 60-71 (1990).

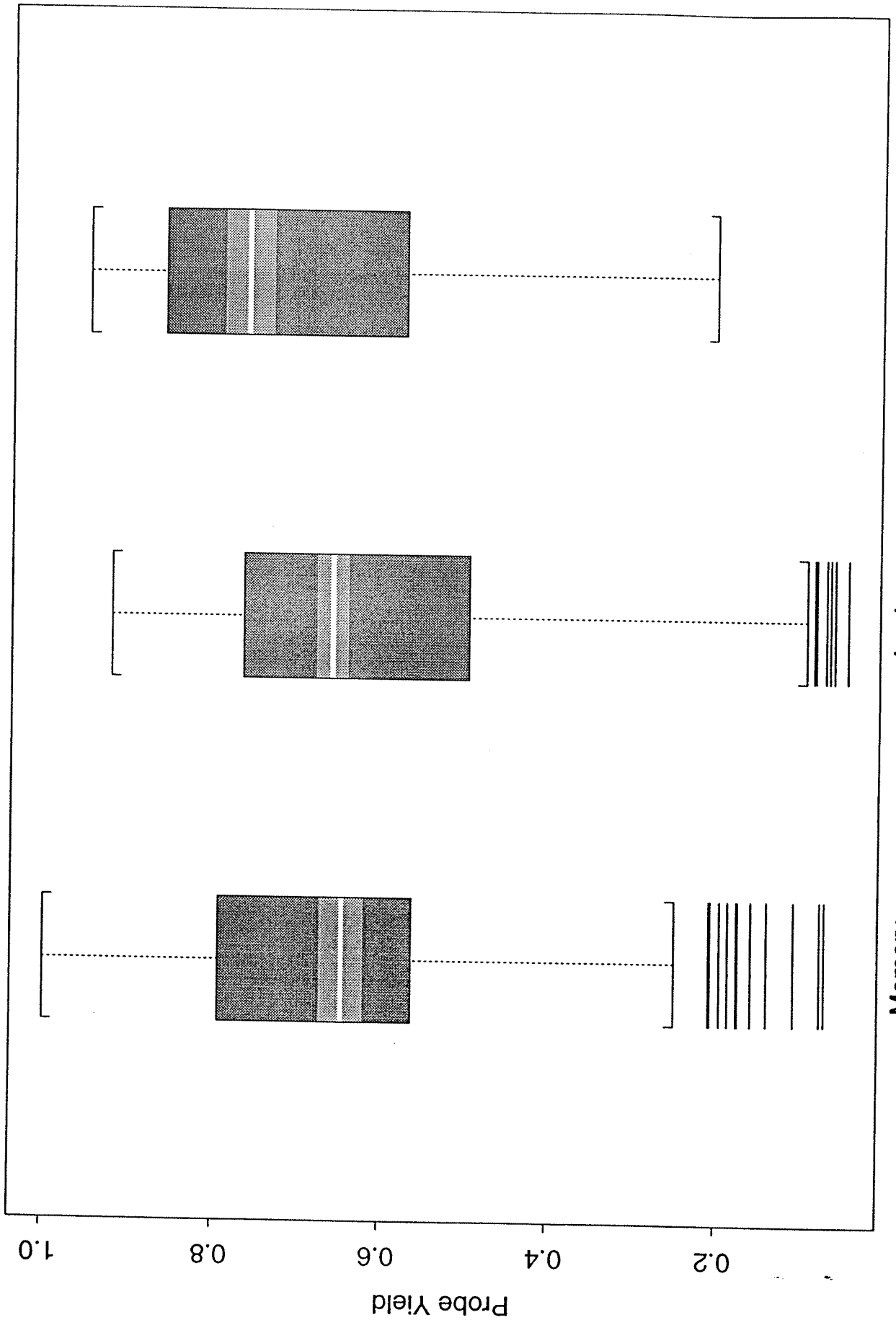


Figure 3.2.2
Boxplot of Die Yield vs. Fab Type

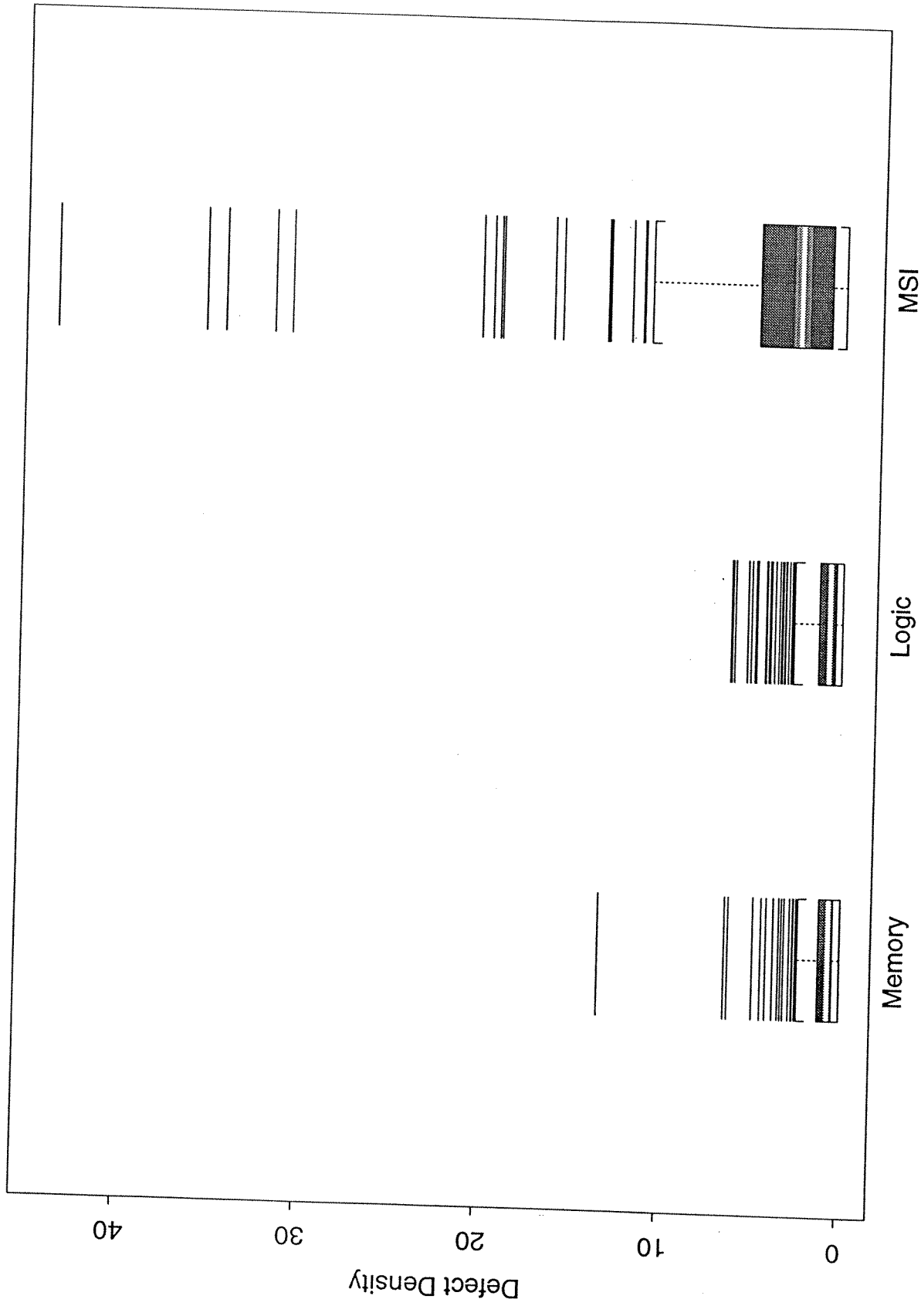


Figure 3.2.3
Boxplot of Defect Density vs. Fab Type

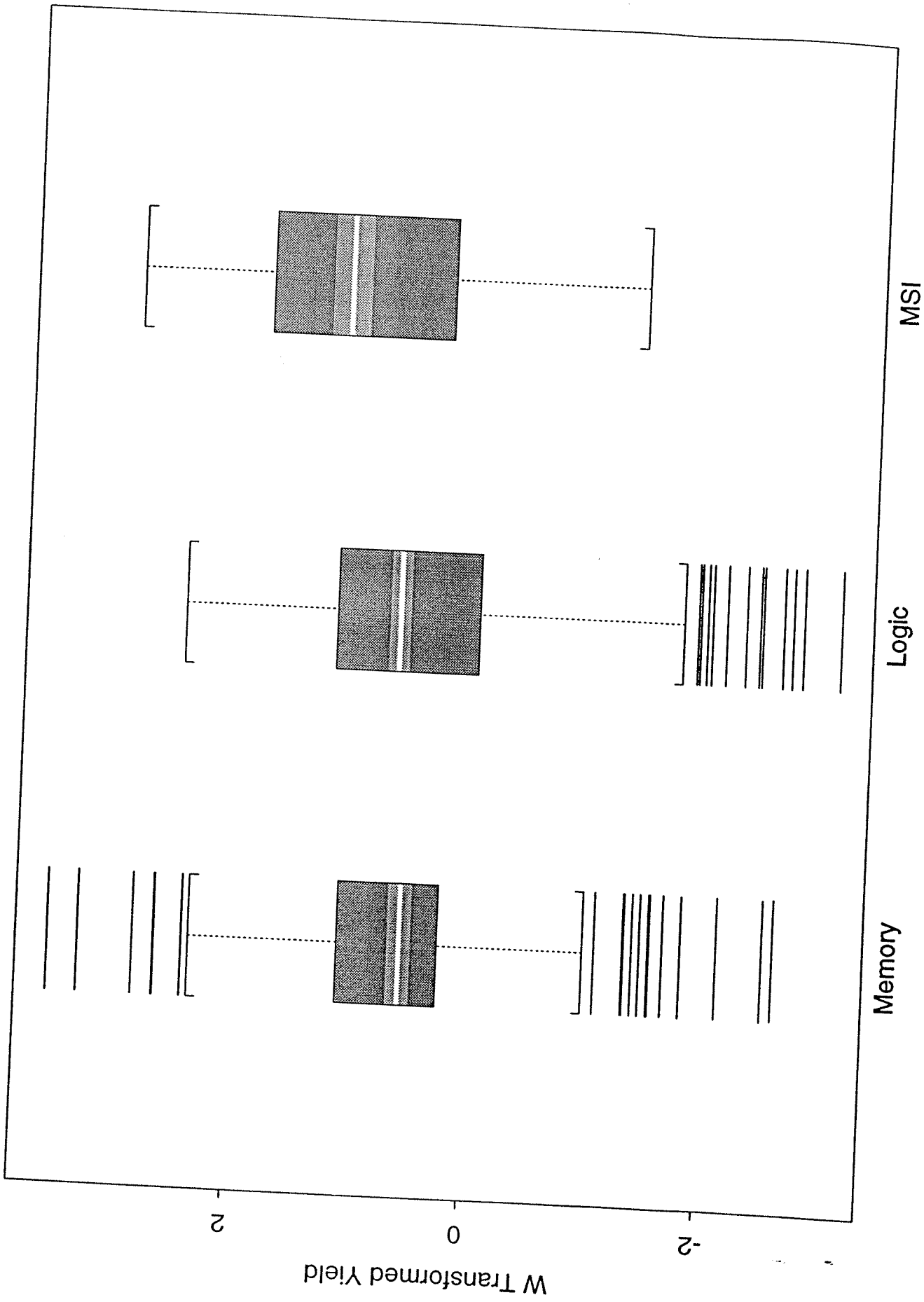


Figure 3.2.4
Boxplot of Transformed Die Yield (W) vs. Fab Type

It is clear that logic and memory fabs have lower defect densities than MSI fabs. However, as mentioned earlier, MSI fabs are not defect limited. MSI fabs tend to have high die yields but also tend to have quite small die sizes. We ended up choosing W as the yield metric to avoid some of the product sensitivity issues mentioned earlier. Table 3.2.2 presents potential explanatory factors for die yield that we analyzed. The die yield figures given for each fab are from the most recent quarter of data for the most advanced technology being operated by the fab at the time of the study.

Our statistical analysis of the complete data set revealed the following three significant process and facility variables:

$$W = 0.84 - 1.29 * DieSize + 0.18 * \log(ProcAge) + 0.24 * (LithoLink)$$

Both the aggregate model and the individual coefficients are significant to greater than a 1% level, yet the model only explains about 31% of the total variation observed. The standard errors for each of the coefficients are as follows:

Constant: (+/- .14)
DieSize: (+/- 0.07)
ProcAge: (+/- 0.03)
LithoLink: (+/- 0.06)

The residuals of the model are plotted in Figure 3.2.5.

Discussion and Conclusions

The analysis of line yield shows a difference in performance between the product type fabs. The first factor which explains the higher line yields in memory fabs is the more recent equipment, including higher levels of automation such as automated recipe download. The second factor is that memory fabs tend to run one or a few die in volume which minimizes the different number of process options and opportunities for human error. The logic fabs tend to be more recent than the MSI fabs but older than memory fabs. MSI fabs are almost all greater than 10 years old and rely on a lot of human input for wafer processing. In addition, MSI fabs tend to have the most diverse product and subprocess options, making manufacturing more challenging.

For line yield it is important to compare fabs within product types. Fabs which consistently excelled in yield seemed to have a sustained, high level of focus in this area. Low yielding fabs usually suffered from a lack of focus or other circumstances such as multiple new processes transferred into production simultaneously.

Die yields tend to be more complicated as they involve a dimension of die design and test which is highly variable across the fabs and die types. The empirical model demonstrated that die size, process age and linked lithography were significant variables, but only sufficient enough to explain 31% of the variation in die yields reported by our participants. This regression agrees with the results found by Cunningham et al [1994]. The fact that product type failed to be significant indicates that a more complex relationship exists between design and die yield. Some

Table 3.2.2. Values of Explanatory Variables for Die Yield Modeling

Fab ID	Die Yield	Process Tech	Die Type	Proc Age	Die Age	Die Size	Fac Size	Fac Class	Fac Age	Litho Type	Litho Link
A1	0.93	0.6u CMOS	Mem	37	37	0.489	2	0	2	Step	0
A2	0.86	2.5u Bipolar	MSI	33	15	0.211	1	2	2	Proj	0
A3	0.66	0.7u CMOS	Logic	28	6	1.142	2	2	2	Step	1
A4	0.91	2.0u Bipolar	MSI	48	30	0.030	2	2	3	Step	1
A5	0.70	0.9u CMOS	Logic	72	63	1.305	2	0	2	Step	1
A6	0.40	0.8u CMOS	Mem	63	21	0.857	3	2	3	Step	0
A7	0.48	0.9u CMOS	Logic	52	39	1.613	3	3	3	Step	1
A8	0.78	0.6u CMOS	Mem	22	12	0.441	3	2	2	Proj	1
A9	0.85	1.5u CMOS	Logic	48	39	0.180	3	1	3	Proj	1
A10	0.68	0.8u CMOS	Logic	24	24	0.448	1	0	1	Step	1
A11	0.53	0.7u CMOS	Logic	33	12	2.271	1	2	3	Step	1
A12	0.22	0.7u CMOS	Logic	17	9	1.914	2	1	2	Step	0
A13	0.45	1.0u CMOS	Logic	18	15	0.800	1	2	3	Step	0
A14	0.64	0.7u CMOS	Logic	9	9	0.760	2	0	1	Step	1
A15	0.56	0.45u CMOS	Mem	5	5	1.020	3	1	1	Step	1
A16	0.54	0.8u CMOS	Logic	30	30	0.129	1	0	2	Step	0
A17	0.46	0.9u CMOS	Logic	31	30	0.700	2	0	1	Step	0
A18	0.44	1.5u CMOS	Logic	76	36	0.523	1	1	3	Step	0
A19	0.60	0.6u CMOS	Mem	13	9	0.372	2	1	2	Step	1
A20	0.47	1.2u Bipolar	MSI	48	48	0.106	2	2	3	Step	0
A21	0.65	0.8u CMOS	Mem	27	27	0.815	2	2	1	Step	1
A22	0.61	0.6u CMOS	Logic	12	6	0.431	2	0	2	Step	0
A23	0.94	0.8u CMOS	Mem	12	12	0.532	2	0	2	Step	0
A24	0.94	5u Bipolar	MSI	14	14	0.051	2	2	3	Proj	0
A25	0.89	1.2u CMOS	Logic	14	14	0.306	2	1	3	Step	0

Notes: *Die Yield* is that reported for the most recent quarter on the most advanced process in production at the time of the survey. *Process Technology* is a description of the process. *Die Type* describes the type of die being produced. *Proc Age* is the age of the process in months. *Die Age* is the length of time in months the die has been in production. *Die Size* is the total area of the device expressed in sq cm. *Fac Size* is an index of the size of the clean room, with 1 indicating less than 20,000 sq ft, 2 indicating between 20,000 and 60,000 sq ft, and 3 indicating greater than 60,000 sq ft. *Fac Class* is the exponent of the rated cleanliness of the clean room (e.g., Fac Class = 1 indicates a class 10 clean room). *Fac Age* indicates how long ago the fab was built, with 1 indicating built in the 1990s, 2 indicating a built during 1985-1989, and 3 indicating built prior to 1985. *Litho Type* indicates the most common photolithography technology used, with *Step* referring to stepper technology and *Proj* indicating projection alignment. *Litho Link* indicates whether the lithography tools (coaters, aligners/steppers, developers) are physically linked together, with 1 indicating they are and 0 indicating they are not.

For reasons of confidentiality, a different numbering scheme for the participants appears in this table.

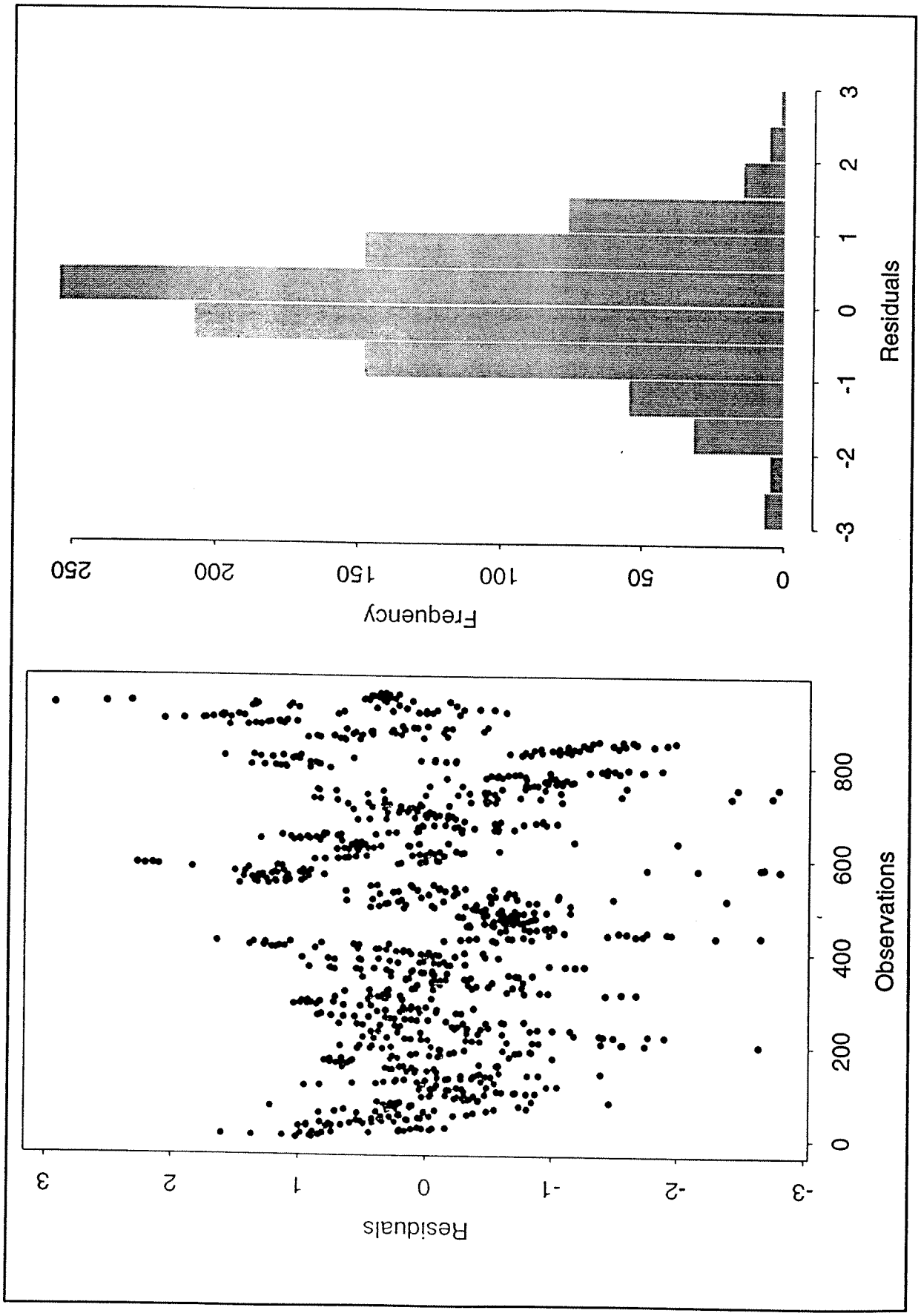


Figure 3.2.5
Boxplot of Die Yield Model Residuals

issues not included in our model but with known impacts on yield include critical die area for given defect size, clustering factors, and product performance specifications.

3.3 Process Control
by George McMurray

The goal of this section is to evaluate the performance of the participant fabs in sustaining and improving process control over time. The results of a study on process control at the 28 participating semiconductor manufacturing facilities are presented. We first examine the statistical stability through time of line yields at each of the wafer fabs, and then list some of the attributes of the SPC systems in use. Our primary method for data collection of these attributes was a discussion on process control held during a site visit with each participant. Typically, this discussion was part of a 90-minute session covering the organizational and technical issues relating to yield improvement and process control. In addition, a tour of the manufacturing clean room provided us with direct observation of statistical process control methods.

It is difficult to determine the level of SPC implementation through the interview session alone. The validation of the SPC programs usually came out in our fab tour. During the fab tour we asked operators to demonstrate SPC data collection and corrective action procedures.

Analysis

We classified the participants into three general categories of fabs: Memory, Logic and MSI. Fabs in the memory group fabricate submicron memory devices, those in the logic group used CMOS process technology to fabricate logic devices with features smaller than 1.5 microns, and those in the MSI group used Bipolar, BiCMOS and CMOS technology to fabricate devices with larger feature sizes. Five of the fabs were fabricating both memory and logic devices while one fab was building both MSI and advanced logic products. Line yields are recorded by fab, so it is was not always possible to separate the product effects in these dual product fabs. The line yields of each of the fabs where analyzed as a time series to evaluate the statistical stability of the line yield. Our goal was to compare the post-start-up phases of line yield, hence the first three quarterly data points were dropped to suppress any start-up problems. This approach was used in lieu of a logarithmic transform of time since it provided an adequate modelling fit.

In a basic evaluation of a run chart, we are interested in any linear trends as well as any outliers that violate the Statistical Control Rules. A first order linear model was used which regressed line yield versus time. For our purposes, positive trends in line yield are not classified as out-of-control (OOC) since they are desirable and are usually the result of a comprehensive process improvement efforts. The residuals of the linear model were analyzed on a X-R chart using a moving range of lag one. The levels of statistical stability are defined by first checking to see if the trend is nondecreasing and then examining if the residuals are in control. Each of the fabs are rated for process control using the following criteria:

High --> Nondecreasing trend and residuals in control
Medium --> Nondecreasing trend but some residuals out of control (OOC)
Low --> Decreasing trend (residuals could be in or out of control)

In cases where single-point outliers changed the rating upwards, the fab was given the benefit of the doubt and the point was deleted. Results are displayed in Table 3.3.1.

A summary of the process control practices at the participants is provided in Table 3.3.2. Most of the fabs prepare similar numbers of charts, and most are automated in the applications of

Table 3.3.1.
Line Yield Performance Evaluation

Fab ID	Rating	Product type	Trend	INC/OOC	No. OOC
M1	High	Mem	3.04	INC	0
M2/L2	High	Mem/Log	0.34*	INC	0
M3/L9	Low	Mem/Log	-1.78	OOC	1/8
M4	High	Mem	1.46	INC	0
M5/L5	High	Mem/Log	14.3	INC	0
M6	Med	Mem	0.90	OOC	1/13
M7/L12	High	Mem/Log	9.44*	INC	0
M8/L14	Low	Mem/Log	-1.12*	OOC	1/10
M9	Med	Mem	1.39*	OOC	1/11
M10	Med	Mem	-0.24*	OOC	1/11
L1	High	Log	3.99	INC	0
L3	High	Log	7.14	INC	0
L4	Med	Log	7.91	OOC	1/14
L6	Med	Log	-0.46*	INC	0
L8	Med	Log	5.82	OOC	2/19
L10	High	Log	6.73	INC	0
L13	Med	Log	2.76	OOC	2/14
L15	Med	Log	5.49	INC	0
L16	High	Log	0.86*	INC	0
B1	Low	MSI	-2.60	INC	0
B2/L7	High	MSI/Log	1.33*	INC	0
B3	Low	MSI	-1.55*	OOC	1/14
B4	Low	MSI	-2.49	OOC	1/19
B5	High	MSI	5.17	INC	0
B6	High	MSI	5.13	INC	0
B7	Low	MSI	-7.41	OOC	1/14
B8	Low	MSI	-3.26	INC	0

Notes: *Product* indicates the type of products fabricated. *Trend* is the slope of the regression of line yield versus time and is significant to a 5% probability level unless marked by an asterisk. *INC/OOC* indicates whether the residuals of the regression model are in control using a Moving Range chart with $n = 2$. *No. OOC* is the ratio of points which are out of control to total data points.

Table 3.3.2.
Process Control Activities at Participating Wafer Fabs

		Practice		Automation		Organization	
Fab ID	Rating	Extent	Visibility	Charts	Action	Training	Owner
M1	High	Standard	Shared	Yes	Yes	Class	Eng
M2/L2	High	Standard	Paper	No	No	OJT	Eng
M3/L9	High	Critical	Paper	No	No	OJT	Mgmt
M4	High	Critical	Paper	No	No	OJT	Mgmt
M5/L5	High	Standard	Dedicate	Yes	Yes	Class	Eng/Team
M6	High	Extensive	Dedicate	Yes	Yes	OJT	Eng/QA
M7/L12	High	Standard	Dedicate	Yes	No	Class	Eng
M9	High	Critical	Paper	No	No	Class	Tech
M10	High	Standard	Dedicate	Yes	Yes	Class	Eng
L3	High	Extensive	Shared	Yes	Yes	Class	Eng/QC
L4	Med	Standard	Shared	Yes	No	Class/OJT	Eng/Team
L6	Med	Standard	Shared	Yes	Yes	Class	Eng
L8	Med	Standard	Shared	Yes	No	Class	Eng
L14/M8	Low	Extensive	Paper	Yes	No	OJT/Team	Eng
L10	High	Extensive	Shared	Yes	Yes	Class	Eng
L11	Med	Standard	Shared	Yes	No	Class	Eng/Teams
L13	Med	Standard	Shared	Yes	Yes	Class	Eng/Mgmt
L15	Med	Standard	Shared	Yes	Yes	Class	Eng/Mgmt
L16	High	Standard	Dedicate	Yes	Yes	Class	Eng/Mgmt
B1	Low	Standard	Paper	No	No	Class	Eng/Mgmt
B2/L7	High	Standard	Shared	Yes	Yes	Class/OJT	Eng
B3	Med	Standard	Dedicate	Yes	Yes	Class	Eng
B5	Low	Critical	Paper	No	No	Class/Team	Tech
B6	High	Critical	Paper	No	No	Class	Tech
B7	Low	Standard	Shared	Yes	No	Class	Eng
B8	Low	Standard	Shared	Yes	No	Class	Eng

Notes: Ratings of the fabs are the same as indicated in Table 3.3.1. *Extent* of SPC practice refers to the volume and placement of SPC charts in the fab. *Critical* indicates the fab primarily monitors critical processes and does not monitor non-critical processes. *Standard* indicates the fab monitors critcal and non-critical processes unequally, usually performing particle monitor checks periodically on non-critical equipment. *Extensive* refers to fabs that maintain very large numbers of control charts for both critical and non-critical processes. *Visibility* refers to the primary source of SPC visibility in the fab. Non-automated fabs rely on paper charts *(Paper),* but more automated fabs have a choice of SPC-dedicated terminals *(Dedicate)* or shared terminals *(Shared),* the latter being the choice in cases where SPC is an add-on module to an existing CAM system. *Action* indicates some form of automated corrective action is utilized, including such features as an automated presentation of corrective action guide lines which appear in a menu following an out of control incident. A negative response indicates absolutely no automation; a positive response indicates limited applications. *Training* refers to the method in which SPC practices are taught within the fab. The amount and nature of SPC training often differs depending on job title, and the training listed here is that received by operators. *Class* indicates the primary form of SPC training is classroom training. *OJT* indicates the primary training occurs via on-the-job training.

Table 3.3.2 (cont.)

Team indicates training is a work team activity, and may consist of OJT and/or class training at the discretion of the work team. *Responsibility* indicates the job title with the ultimate responsibility for SPC, including updates to procedures, training, and control charts kept. *Eng* indicates engineering personnel; *Mgmt* indicates production management; *Techs* indicates technicians; *Teams* indicates operator-led SPC teams and QC circles; other acronyms *(QC,QA)* indicate engineering-led quality initiatives.

Charting and Action. Training is typically done in a class room setting with various course levels for operators, technicians and engineers. The organizational responsibility of SPC was sometimes difficult to determine though it appeared mostly to reside at the engineering level. Fabs with very good Process Control were actively empowering the operators and technicians to take ownership of SPC, maintaining the charts and carrying out the out-of-control action procedures (OCAPs).

Discussion

The MSI fabs seemed to have weaker process control as a group, with five out of eight fabs exhibiting decreasing trends. This could be due to a wide range of business factors and historical issues, such as the age of the equipment sets, a larger number of process flows run within the fab, and changing volumes and product mixes. The MSI products are usually older products with large device feature sizes and so tend not to be evolving with as fast a pace of new process technology introduction as in the memory and logic fabs. However, process control for analog and bipolar products is in general more difficult than for CMOS digital products. It is thus prudent to compare line yields of fabs within groups.

Fabs dedicated to either logic or memory performed much better. Only one out of the eleven pure logic fabs exhibits decreasing trends in line yields. All pure memory fabs had positive trends, probably a result of competitive pricing pressures as well as a minimal number of products and process flows. With fewer products per process flow and fewer process flows, the fabs can attain higher line yields due to product mix consistency as well as designing process flows to optimize specific products. Out of the five fabs running both logic and memory flows, two exhibit decreasing trends in line yields, while the single fab running both MSI and logic devices had an increasing trend.

In previous studies we have equated statistical process control (SPC) with process control (PC) when in reality SPC is a subset of PC. This distinction is important for there are several fabs new to the study which have achieved very good process control (as inferred through line yield) via extensive in-line defectivity inspection. One of the objectives of SPC is to continuously improve processes and reduce the need for inspection. The in-line inspection programs we observed were mostly oriented toward crisis containment rather than root cause elimination. Thus these fabs were achieving high levels of process control through extensive in-line inspection sampling. Good CIM capability seemed not to be a necessary condition for high level of process control. One of the best performing fabs turned out to have weak CIM system; however, this fab also had a very narrow product/process scope.

Conclusions

We have listed some of the common attributes of SPC programs among the fabs. Using line yield as an aggregate metric of process control we evaluated the statistical time stability of line yields at the fabs. The memory fabs were able to run the highest levels of process control. The logic fabs were a close second, while fabs which were trying to build two product types tended to have less successful process control. The MSI fabs performed much more poorly than the other two categories. We attribute this to the age of the fabs and equipment as well as the peculiar challenges in analog and bipolar products. It appears that the economic incentives for keeping pace with process and equipment technology upgrades was not felt to be warranted by fabs in the

MSI product category. It is still unclear why so many MSI fabs had negative trends instead of no trends. Perhaps the equipment sets were being pushed more and more beyond the original design capabilities.

In the more advanced memory and logic fabs, in-line tools such as particle detection equipment were extensively utilized to achieve very high process control and yield. However the use of the inspection tools were mostly used for crisis containment as opposed to root cause elimination. With a proper focus on Process Control, high levels of improvement and statistical control are possible without sophisticated CIM systems in fabs with narrow product/process scopes. However, as fabs expand in their product/process scope, it seems that a good CIM system helps to manage the higher levels of complexity.

3.4. Equipment Efficiency Improvement
by Robert C. Leachman

The figures in Chapter 2 display a remarkable disparity in the achieved throughputs for 5X steppers, ion implanters and metallization machines. While many of our participants now achieve very competitive yields, there seems to be greater disparity in equipment throughput. This suggests that equipment throughput may be replacing yield as the most significant discriminator of product cost.

Losses of potential equipment throughput may be classified into three basic categories. First, equipment may be unavailable for processing work because of maintenance, repairs, cleaning, changeovers, engineering work or waiting for same. These represent losses of equipment *availability.* All of our participants measure equipment availability, or more precisely, they track and record nonavailable time. There is some variation from fab to fab in the quality of equipment tracking, particularly whether or not short-duration losses are recorded, such as the time required to adjust the machine to perform a different recipe.

Second, the equipment may be available for processing but no processing activity is underway, because no WIP is at hand, or WIP is at hand but no operators are available, or WIP controls inhibit processing effort, or a process hold is in effect because an out-of-control measurement has been recorded. Such idle periods represent losses of equipment *utilization.* In general, there is some trade-off between equipment utilization and allowed WIP level in the fab. Fabs very concerned about cycle time may choose to keep a lower WIP level than those most concerned about product cost. For example, one might expect a lower level of equipment utilization at an ASIC fab than at a memory fab.

The final kind of loss occurs when the equipment is engaged in processing activity, but the processing rate is slower than theoretical machine capability because of machine jams, rework, test runs, delays waiting for inspection results, or internal machine speed losses arising from power supply or gas flow deficiencies, inferior optical paths, mechanical problems, etc. These represent losses of machine *rate efficiency.* An important component of this loss is the time required to set up equipment to run the next lot and recipe (including time for test runs), if such time is not included in the reported availability losses.

The overall machine efficiency may be thought of as the product of equipment availability, the utilization of available time, and the rate efficiency. It is of interest to ascertain how much of the disparity in equipment throughputs may be attributed to losses in each of the three categories. Towards this purpose, we have prepared graphs of reported availability for each of the three equipment types, as reported by the participants. Figures 3.4.1 - 3.4.14 placed at the end of this section show trends in reported availability for 5X steppers, ion implanters and metallization machines at the three kinds of fabs (memory, logic and MSI).

Availability trends for 5X steppers have been graphed for G-Line steppers and the newer I-Line steppers in Figures 3.4.1 - 3.4.5. As can be seen, many fabs achieve nearly identical availability scores in the low 90s, yet their 5X stepper throughputs shown in Figures 2.8, 2.28 and 2.36 are much more disparate. The relatively high availability common to many fabs does not explain the variance in stepper throughput; in fact, a statistical correlation analysis of the 5X stepper throughputs with the availabilities reported by our participants reveals a slight *negative*

correlation.

As indicated in Tables 2.1 - 2.3, most of the participants load their fabs to capacity, and most have the 5X steppers as their limiting equipment resource. Thus differences in reported utilization do not seem to provide most of the explanation for differences in stepper throughputs, either. The primary differentiator of stepper throughput would seem to be rate efficiency. In particular, time the steppers spend idle waiting for the results of inspections of sample wafers is a key factor underlying performance.

Turning to ion implanters, Figures 3.4.6 - 3.4.11 show availability trends for high current and medium current ion implant machines at the participants. In the case of this machine type, the disparities in availability are substantial. Implanters are very complicated machines for which substantial expertise is required to achieve high availability. In our site visits, we found that the time required to change over these machines to implant a different species and the time required to replace a depleted species gas bottle varied substantially among the participants. A correlation analysis shows that about 37% of implanter throughput variance among our participants is explained by variation in availability.

This relationship is even stronger for metallization machines, as a correlation analysis shows that about 44% of the variation in metallization throughput among our participants is explained by the variation in availability. Metallization machine availability trends are shown in Figures 3.4.12 - 3.4.14.

Availability is a function of the response time of the fab staff to restore equipment to good working order. In most fabs, equipment maintenance is the primary responsibility of equipment technicians. Many of our participants have asked for a comparison of the number of technicians per machine. The participants report the total number of technicians employed at the fab (including both process technicians and equipment technicians, and also including equipment vendor technicians dedicated to the fab), and they report their inventory of major types of processing equipment. We have computed a simple ratio of the number of processing machines per technician from these data for each fab. The results are displayed in Figures 3.4.15 - 3.4.17 placed at the end of this section.

As can be seen, most CMOS logic fabs and MSI fabs staff to a level of about two machines per technician. Some of the older or smaller fabs operate with one machine per tech. However, one CMOS logic fab and three memory fabs report substantially more machines per tech. Fabs M2, M4 and M6 do not have any equipment maintenance technicians; their duties have been consolidated with those of operators and equipment engineers. At these fabs, operators receive considerable training in equipment maintenance.

Considering the differences in job classifications at various fabs, we have also studied the total fab headcount per processing machine, as graphed in Figures 3.4.18 - 3.4.20 placed at the end of this chapter. Most memory fabs staff to a level of 1-2 persons per machine, but a couple of fabs (M3 and M8) report the much higher level of 3.4 persons per machine. These latter two fabs have much a higher number of die types in production, as they also produce a diverse set of logic products. Staffing levels at CMOS logic fabs are more disparate. One group of 8 fabs reports about 1.5-2.5 persons per machine, another group of four fabs employs 3-4 persons per machine, and four other ASIC fabs report a high level of 5-7 persons per machine. At MSI fabs, three

report 1.5-2.5 persons per machine, four other MSI fabs report 3-4 persons per machine, while one MSI fab seems to be out of control, climbing to 6 persons per machine.

To identify the key practices for achieving high equipment efficiency, the scores for equipment throughput and availability were correlated with indices representing factors such as the amount of staffing, training, data collection, and equipment vendor support, as well as with general fab characteristics such as volume and workload. Tables 3.4.1 - 3.4.3 display these indices for the three categories of fabs. The indices (high, medium, low) shown in the tables represent our judgements based on our site visit interviews with the participants. The various practice categories are briefly explained as follows, classified into groups for data collection, training, equipment improvement efforts, maintenance strategy.

In the data collection group, practices include the tracking and Pareto analysis of equipment "down" (nonavailable) time, equipment utilization, setup time and overall efficiency (OEE). Nonavailable time is easiest to track, and almost all fabs we have studied are mature in this area. Utilization is more difficult to track, but such data allows fabs to investigate and reduce idle time losses on bottlenecks. As discussed above, setup times (i.e., times required to change over to a different machine recipe or to start up another machine run) are particularly significant for 5X steppers, yet hardly any fabs are skillfully tracking and analyzing such losses. Tracking overall efficiency (OEE) requires the most sophistication and is most revealing about losses in equipment productivity. Most fabs rely on manual systems to capture equipment performance data, but a few leaders use SECSII interfaces to directly capture machine logs and summarize such data into a useful form. Fab M4 reports that it now automatically captures performance data for 100% of its major processing equipment. The "auto-monitoring" category refers to the use of sensors and timers to monitor equipment operation and to automatically set off alarms or notifications when something about the equipment is awry (e.g., processing cycle taking too long, process aborted, etc.). Finally the "compare with other fabs" category indicates the extent to which the fab regularly compares equipment performance data with performance data from other fab lines.

In the training category, there are items for training of technicians and operators by equipment vendors. Only fab M6 has carried out extensive training of their operators by equipment vendors. There are also items in this category for the amount of training of technicians and operators in TPM (total productive maintenance). For operators, this involves training by technicians or engineers to perform all light maintenance and trouble-shooting; for technicians, this involves training by engineers to take over equipment management, to understand fundamental equipment improvement issues, and to thoroughly document equipment conditions and procedures.

In the equipment improvement category, there is an item for the staffing level of equipment engineers, and another item for how merged are the equipment and process engineering organizations. There is an item for the intensity of use of continuous improvement teams (CITs) consisting primarily of technicians and operators, and another for the intensity of use of CITs consisting primarily of engineers and technicians. Typically, both kinds of teams are organized under the TPM paradigm, and are focussed on developing and carrying out projects to increase machine throughput. There is a practice item for the intensity and frequency of modifications to equipment already installed in the fab, typically in connection with TPM program CIT efforts. Such improvements include replacement of wet pumps with dry ones, improvements in wafer transport mechanisms to reduce trouble, various rearrangements or modifications to panels, gas lines,

Table 3.4.1 Summary of Equipment Practices at Memory Fabs

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
Data Collection										
Track down time	H	H	H	H	H	H	H	H	H	H
Track utilization	H	H	H	H	H	H	M	L	H	H
Track setup time	L	L	H	H	L	M	L	L	L	L
Track OEE	L	M	L->M	M->H	L	M	L	L	L	H
Auto-capture perf. data	L	H	L	M->H	L	M	L	L	L	L
Auto-monitoring	L	H	L	M->H	L	M	L	L	L	L
Compare w/ other fabs	H	M	M	M	L	H	M	L	M	H
Training										
TPM training of techs	L	H	H	H	L	H	L	L	M	H
Vendor school for techs	L	M	L	L	M	H	H	L	M	L
TPM training of oprs	L	H	H	M	L	H	L	L	M	H
Vendor school for oprs	L	L	L	L	L	H	L	L	L	L
Eqpt improvement										
No. of eqpt. engineers	L	H	H	L	H	H	L	H	L	H
Joint. proc. & equip. engrng.	L	M	M	M	H	L	M	L	H	L
CIT tech/opr teams	L	M	H	M	L	H	L	L	M	M->H
CIT eng/tech teams	M	M->H	H	H	M	H	M	H	M	H
Eqpt modifications	L	M	H	H	H	H	M	M	L	H
Share mods w/ other fabs	H	L	H	H	L	H	H	L	L	H
TPM 5 S	L	H	H	H	L	H	L	L	L	M->H
Setup time reduction	L	L	L	L	H	H	L	L	L	L
Mtce strategy										
No. of techs per machine	H	NA	H	NA	L	NA	M	H	M	M
Eqpt owner program	L	L	M	M	L	H	L	H	L	L
Opr mtce	L	M	M	M	L	H	L	L	L	M
Vendor contract mtce	L	L	L	L	L	L	L	L	M	L
Nearby on-call vendors	H	H	H	H	L->M	M	H	L->M	H	H
Reg vendor reviews	M	M	M	M	H	H	H	H	M	M
Coord rev w/ other fabs	H	L	M	M	L	H	H	L	L	H
Fab characteristics										
Factory utilization	H	H	H	H	H	H	H	H	H	H
Wafer starts per week	5,400	10,000	15,000	12,000	7,800	8,000	2,000	7,200	1,200	13,000
No. of process flows	1	4	55	3	3	3	9	3	2	7
No. of active die types	6	80	320	12	40	15	85	140	3	10
Bottleneck eqpt type	PE	S	S	S	S	S/Imp	Dif	S	S	S
Eqpt. availability										
5X stepper availability	M->H	M	L	H	M	NA	H	H	M->H	H
Implanter availability	M/L	NA	M	M	L/M	NA	H	H	M	M
Metallization availability	M	NA	H	M	M	NA	M->H	H	NA	L->M
Eqpt. throughput										
5X stepper throughput	L	M->H	M	H	H	H	L	M->H	M	M->H
Implanter throughput	M	M	H	M	M	H	M	M->H	L	M
Metallization throughput	L	M	H	M	H	M	M	H	NA	M

Abbreviations: L - low, M - medium, H - high, NA - no data, PE - plasma etch, S - 5X stepper, Imp - high current ion implanter, Dif - diffusion.

Table 3.4.2 Summary of Equipment Practices at CMOS Logic Fabs

	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
Data Collection																
Track down time	H	H	H	M	H	H	H	H	H	H	H	H	H	H	H	M
Track utilization	H	H	L	M	H	M	H	H	H	L	M	M	H	L	H	L
Track setup time	L	L	L	L	L	H	M	L	M	L	L	L	L	L	L	L
Track OEE	M	M	L	L	L	L	L	L	L->M	L	L	L	L->M	L	L	L
Auto-capture perf. data	L	H	L	L	L	L	L	L	L	L	L	L	M	L	L	L
Auto-monitoring	L	H	L	L	L	L	L	L	L	L	L	L	M	L	L	L
Compare with other fabs	L	M	H	L	L	H	L	H	M	H	L	M	H	L	M	H
Training																
TPM training of techs	L	H	L	L	L	L	L	L->H	H	L	L	L	M	L	L	L
Vendor school for techs	L	M	H	M	M	M	L	H	L	H	M	L	H	L	M	H
TPM training of oprs	L	H	L	L	L	L	L	L->H	H	L	L	L	M	L	L	M
Vendor school for oprs	L	L	L	L	L	L	L	L->M	L	L	L	L	M	L	L	L
Eqpt improvement																
No. of eqpt. engineers	L	H	M	M	H	L	L	L	H	L	L	L	L	H	L	L
Joint proc. & eqpt. engrng.	L	M	H	L->H	H	L	L	H	M	L	L	M	L	L	L	L
CIT tech/opr teams	L	M	L	L	L	L	L	L->H	H	M	L	L	L->M	L	L	M
CIT eng/tech teams	M	M->H	H	H	M	L	L	L	H	H	M	M	L->M	H	M	L
Eqpt modifications	M	M	M	M	H	M	L	M	H	M	L	M	L->M	M	L	H
Share mods w/ other fabs	H	L	H	H	L	M	L	H	H	H	L	H	M	L	L	M
Setup time reduction	L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L
TPM 5 S	L	H	L	L	L	L	M	L	H	L	H	L	L	L	L	L
Mtce strategy																
No. of techs per machine	H	NA	H	M	L	H	H	H	M	H	H	L	H	M	H	M
Eqpt owner program	L	L	M	L	L	L	L	M->H	M	L	H	L	H	H	L	L
Opr mtce	L	M	L	L	L	L	L	L	M	L	L	L	L	L	L	M
Vendor contract mtce	L	L	M	M	L	M	L	M	L	M	L	L	M	L	M	L
Nearby on-call vendors	L	H	M	H	L->M	H	L	M->H	H	M	H	H	M	L->M	L	H
Reg vendor reviews	H	M	H	H	H	M	H	H	M	H	H	M	L->M	H	L	H
Coord rev w/ other fabs	L	L	H	H	L	L	L	H	M	H	H	H	M	H	L	H
Fab characteristics																
Factory utilization	M	H	H	H	H	M	H	H	H	L	M	H	H	H	H	H
Wafer starts per week	4,800	10,000	600	3,000	7,800	5,500	3,300	4,500	15,000	300	1,900	2,000	4,200	7,200	2,500	6,600
No. of process flows	5	4	2	4	3	12	10	1	55	2	7	9	5	3	3	3
No. of active die types	85	80	13	50	40	200	400	5	320	10	600	85	150	140	15	50
Bottleneck eqpt. type	M	S	M	S	S	S	PE	S	S	Dif	S	Dif	Dif	S	S	S
Eqpt. availability																
5X stepper availability	H	M	M	H	M	M	H	M	L	H	H	H	H	H	M	H
Implanter availability	M	NA	L	H	L	L	M->H	H	M	NA	NA	M	M	M	L	M
Metallization availability	M	NA	L	L	M	NA	M->H	H	M	M	L->M	M->H	H	M	L	M
Eqpt. throughput																
5X stepper throughput	M	H	L	L->M	H	M	H->M	H	H->M	L	L	M	M	H	M	M
Implanter throughput	L->H	H	L	M	M	M	L	H	H	NA	NA	M	L	M->H	L	L
Metallization throughput	M	L	L	M	M->H	M	M	H	M	L	M	M	M	H	L->M	M

Abbreviations: L - low, M - medium, H - high, NA - no data, Met - metallization, S - 5X stepper, PE - plasma etch.

Table 3.4.3 Summary of Equipment Practices at MSI Fabs

	B1	B2	B3	B4	B5	B6	B7	B8
Data Collection								
Track down time	L	H	H	H	H	H	M	M
Track utilization	L	H	H	L	L->H	L	M	M
Track setup time	L	M	L	L	L	L	L	L
Track OEE	L	L	L	H	L	L	L	L
Auto-capture perf. data	L	L	L	L	L	L	L	L
Auto-monitoring	L	L	L	L	L	L	L	L
Compare with other fabs	L	L	L->M	M	L	L	M	M
Training								
TPM training of techs	L	L	L	H	M	L	L	L
Vendor school for techs	L	L	M	M	M	M	H	H
TPM training of oprs	L	L	L	M->H	L	L	L	L
Vendor school for oprs	L	L	L	L	L	L	L	L
Eqpt improvement								
No. of equip. engineers	L	L	L	L	L	L	L	L
Joint proc. & eqpt. engrng.	L	L	H	L	L	L	L	L
CIT tech/opr teams	L	L	H	H	L	M	L	L
CIT eng/tech teams	L	L	H	H	M->H	M	L	L
Eqpt modifications	L	L	H	M	L	L	L	L
Share mods w/ other fabs	M	L	M->H	M	L	L	L	L
TPM 5 S improvements	L	M	L	M->H	L	L	L	L
Setup time reduction	L	L	H	L	L	L	L	L
Mtce strategy								
No. of techs per machine	L->M	L->H	H	L	M	L	H	H
Eqpt owner program	L	L	L	L	M->H	L	L	L
Opr mtce	L	L	L	M->H	L	L	L	L
Vendor contract mtce	L	L	M	L	M	L	M	M
Nearby on-call vendors	L	L	H	M	M	M	M	M
Reg vendor reviews	M	H	M	L	M	M	M	M
Coord rev w/ other fabs	H	L	L->M	M	L	L	L	L
Fab characteristics								
Factory utilization	H	H	H	H	H	L	H	H
Wafer starts per week	2,800	3,300	11,000	900	1,800	2,600	2,000	11,000
No. of process flows	3	10	6	4	3	10	5	5
No. of active die types	65	400	180	61	45	212	200	130
Bottleneck eqpt type	S	CVD	S	C	C	PE	PA	PA
Eqpt. availability								
5X stepper availability	NA	H	H	NA	NA	NA	NA	NA
Implanter availability	M	M	H	L	H	M	L	M
Metallization availability	H	M	M	H->L	L->H	M	L	L
Eqpt. throughput								
5X stepper throughput	NA	M	H	NA	NA	NA	NA	NA
Implanter throughput	L	M->L	H	L	L	M->L	L	M->L
Metallization throughput	L	H->L	H	L	NA	L	L	L

Abbreviations: L - low, M - medium, H - high, NA - no data, S - 5X stepper, C - coat track, PE - plasma etch, PA -projection aligner.

chambers and assemblies to reduce difficulty of maintenance, etc. A related item in this category indicates the extent to which modification efforts are shared among multiple fabs, whereby one fab can pilot a modification on behalf of several fabs. Another category concerns the extent of TPM "5 S" improvements, involving a general organizing of the equipment area and procedures, including a thorough machine inspection and labelling of parts, putting maintenance and operating documentation in good order and making it accessible, organizing storage and accessibility of tools, etc. The final practice in this category concerns the extent of effort in setup time reduction.

In the category for maintenance strategy, the first item is for the staffing level in the fab of technicians. The second item concerns whether or not there is an "equipment ownership" or "key man" program, whereby a technician or operator expert for each equipment type is resident every operating shift in the fab. This expert can be turned to by other staff with questions and has ownership of equipment maintenance and operating procedures and documentation. The third item concerns the level of operator maintenance in the fab. The fourth concerns the level of contract vendor maintenance, and the fifth indicates the degree to which there exists nearby offices of equipment vendors who can respond quickly for on-call service. The sixth index in this category indicates the frequency of performance reviews with equipment vendors, and the last index indicates the extent to which vendor reviews are coordinated with other fabs in the same company.

For convenience, the fab characteristics category included in each table replicates information from Tables 2.1 - 2.3 concerning factory size, utilization, number of process flows, number of die types, and which equipment type is the bottleneck. At the bottom of each table, indices concerning fab performance in availability and throughput of 5X steppers, ion implanters and metallization machines have been recorded, whereby the numerical scores for each fab type have been given into high, medium and low classifications. In some instances, participants made transitions in their practices or performance during the time frame of their performance data reported to us; for example, "M->H" indicates the fab transitioned from medium to high intensity or performance. In all fairness, it must be acknowledged that many of our participants had upgraded their equipment-related practices considerably at the time of our site visit, but we report here our judgement of their equipment practices during the time frame of their performance data.

Table 3.4.4 displays the results of correlation analysis between the practices and equipment performance. Also displayed are correlations between fab characteristics and performance. Correlations greater than 0.35 are shown in bold face; correlations between 0.25 and 0.35 are italicized; while correlations smaller than 0.2 are left in plain type.

Considering fab characteristics, equipment availability is not correlated with fab size or workload, but equipment throughput is strongly correlated with fab size and focus. The large fabs and those with a large number of wafer starts per process flow and a large number of wafer starts per die type achieve the highest throughputs. There clearly is a handicap in equipment throughput for small fabs. A smaller but still significant handicap seems to exist for fabs with a variety of process flows and die types.

Turning to correlations between practices and performance, we find few positive correlations concerning reported equipment availability. Holding regular reviews with equipment vendors, and the existence of an equipment ownership program show the highest positive correlations. Both of these practices tend to promote quicker and more effective response to equipment problems.

Table 3.4.4
Correlation Coefficients for Equipment Practices vs. Equipment Performance

Practice	Equipment Performance					
	Stepper avail.	Implanter avail.	Metal avail.	Stepper t'put	Implanter t'put	Metal t'put
Data collection						
Track down time	-0.221	-0.011	0.127	0.171	*0.342*	*0.336*
Track utilization	-0.323	0.040	0.059	**0.407**	**0.349**	*0.316*
Track setup time	-0.331	-0.108	0.233	0.170	*0.267*	0.210
Track OEE	-0.017	-0.167	-0.013	**0.347**	0.150	-0.112
Auto-capture perf. data	-0.087	0.007	0.164	**0.352**	0.231	-0.103
Auto-monitoring	-0.087	0.007	0.164	**0.352**	0.231	-0.103
Compare with other fabs	-0.168	-0.273	-0.028	-0.216	0.057	-0.242
Training						
TPM training of techs	-0.454	0.016	0.200	**0.415**	**0.345**	0.036
Vendor school for techs	0.007	-0.071	-0.266	-0.213	-0.198	-0.241
TPM training of oprs	-0.481	-0.021	0.226	**0.374**	**0.384**	0.064
Vendor school for oprs	0.064	0.136	**0.406**	0.232	0.222	0.096
Eqpt improvement						
No. of equip. engineers	-0.478	-0.044	0.047	**0.467**	**0.572**	**0.399**
Joint proc. & eqpt. engrng.	-0.405	0.085	0.052	*0.253*	*0.323*	**0.405**
CIT tech/opr teams	-0.368	0.089	0.187	**0.363**	**0.441**	0.107
CIT eng/tech teams	-0.110	0.133	-0.110	0.076	**0.448**	0.167
Eqpt modifications	-0.272	0.030	0.143	**0.493**	**0.604**	**0.537**
Share mods w/ other fabs	-0.018	0.174	0.151	-0.274	**0.373**	0.027
TPM 5 S improvements	-0.148	-0.089	-0.070	*0.254*	0.225	0.166
Setup time reduction	-0.208	0.135	-0.052	*0.322*	**0.505**	0.186
Mtce strategy						
No. of techs per machine	0.008	0.114	-0.084	-0.315	0.117	0.011
Eqpt owner program	0.000	*0.309*	*0.309*	0.144	*0.300*	**0.412**
Opr mtce	-0.361	-0.162	0.048	**0.371**	*0.312*	-0.042
Vendor contract mtce	-0.021	0.020	-0.428	-0.231	-0.270	-0.055
Nearby on-call vendors	-0.146	0.192	-0.042	-0.161	**0.374**	0.057
Reg vendor reviews	**0.395**	**0.357**	0.158	-0.107	0.231	**0.395**
Coord rev w/ other fabs	0.094	0.174	0.069	-0.420	0.191	-0.157
Fab characteristics						
Factory utilization	-0.178	0.112	0.061	**0.427**	0.046	*0.279*
Wafer starts per week	-0.445	0.100	0.103	**0.605**	**0.665**	**0.410**
Wfr strts per proc flow	-0.115	0.091	0.178	**0.440**	**0.476**	*0.292*
Wfr strts per die type	0.047	0.036	-0.003	*0.239*	*0.231*	0.088

In contrast, we find many more positive correlations with respect to equipment throughput, perhaps reflecting the great dispersion of throughput performance. The highest correlations with equipment throughput in Table 3.4.4 are registered for the number of equipment engineers and the intensity of equipment modifications. High correlations also show up for merging process and equipment engineering organizations, TPM training of technicians and operators, intensive use of CITs of techs and operators, operator-performed maintenance, equipment ownership programs, and with careful tracking of utilization and down time.

In the data collection category, positive correlations show up for all categories except comparison with other fabs in the same company. Tracking down time well is significant for implanters and metallization machines, perhaps reflecting the fact that availability losses are still large for these machines. Tracking utilization is important for steppers and implanters, while tracking setup time seems most significant for implanters. Tracking OEE, auto-capture of performance data and auto-monitoring show up most strongly for stepper throughput, perhaps reflecting the fact that steppers are typically the bottleneck.

At first glance, it may seem contradictory that tracking down time is not correlated with reported availability, yet it is correlated with calculated throughput. We believe the reason is that, as the proficiency of down time tracking is increased, the capture and recording of events of nonavailable time also is increased. Thus *reported* availability may decline with improved tracking capabilities. But this increased visibility to losses of efficiency can lead to increased problem-solving activity and higher throughput.

In the training category, TPM training of both operators and technicians seems quite effective, while vendor training of techs does not distinguish fab performance. Vendor training of operators is more positive, but we have only one participant (with high throughput scores) who reports such a practice.

In the equipment improvement category, fabs with strong equipment engineering groups able to identify and undertake many useful modifications are able to achieve superior equipment throughput. While such modifications may be carried out by vendor staff or jointly with vendor staff, the presence in the organization of equipment talent able to identify the need for and direct such improvements seems to be key. Integration of process and equipment engineering groups seems to be beneficial, as does the integration of manufacturing and engineering staff through the deployment of continuous improvement teams (CITs). For the difficult technical problems associated with ion implanters, teams of technicians and engineers working on setup time reduction are beneficial, as are alliances with other fabs. Setup time reduction efforts with respect to 5X steppers also distinguish fab performances.

With respect to maintenance strategy, equipment ownership programs and operator-performed maintenance are most significant. Support from nearby vendor offices for implanters is significant, while the practice of holding regular vendor reviews is most significant for metallization machines.

In summary, the leading fabs have considerable in-house equipment engineering talent, identifying and implementing useful modifications to process equipment that improve performance or ease maintenance. Rather that being a stand-alone organization, equipment engineering is closely integrated with process engineering. Equipment performance is rigorously tracked and

analyzed. Operators and technicians are trained in TPM methods and participate extensively in continuous improvement teams. Operators handle all minor maintenance, and TPM "5 S" improvements have been made. Equipment owners or "key men" are on duty every shift, insuring prompt response to equipment problems.

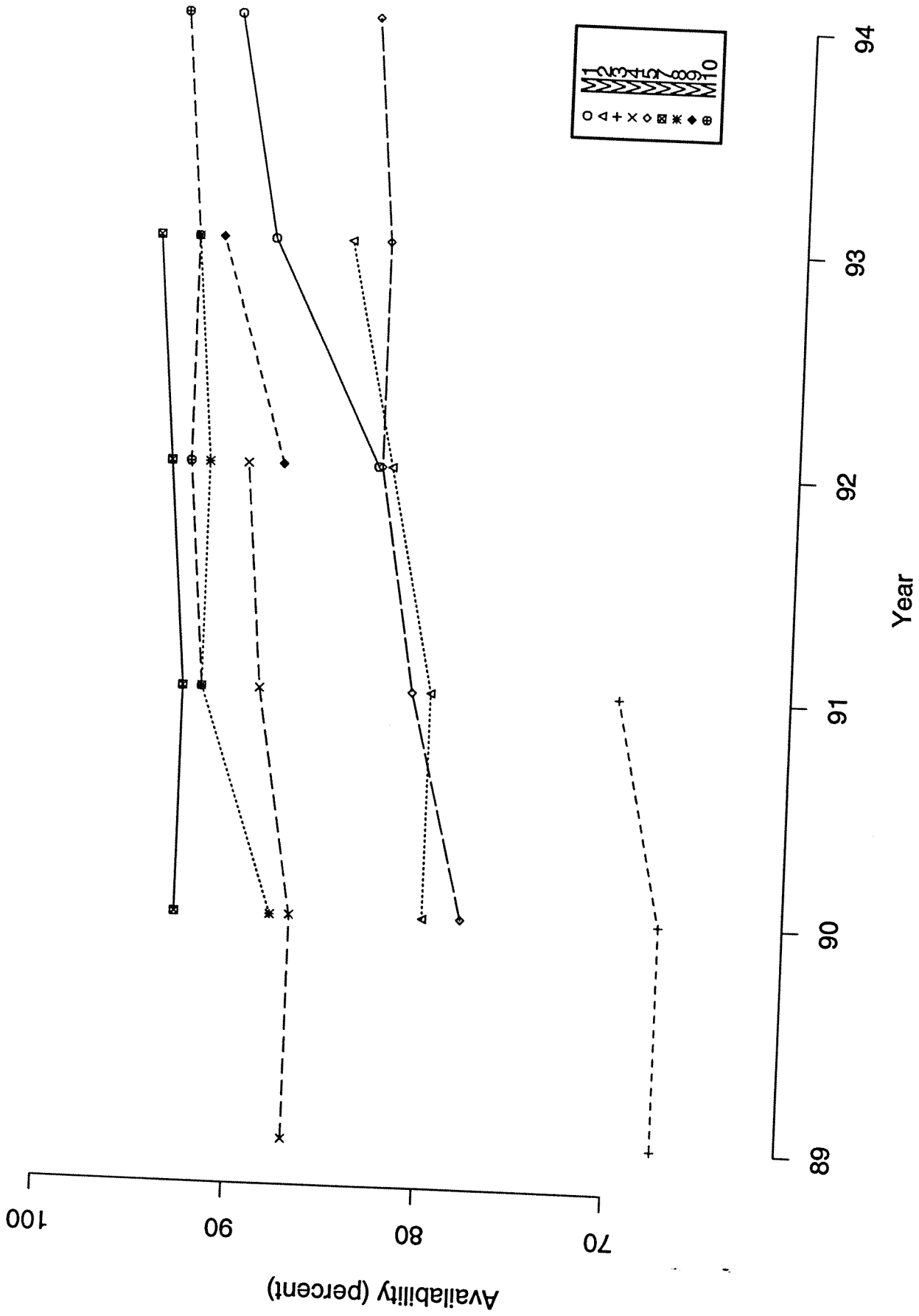


Figure 3.4.1. Availability of G Line Steppers at Memory Fabs

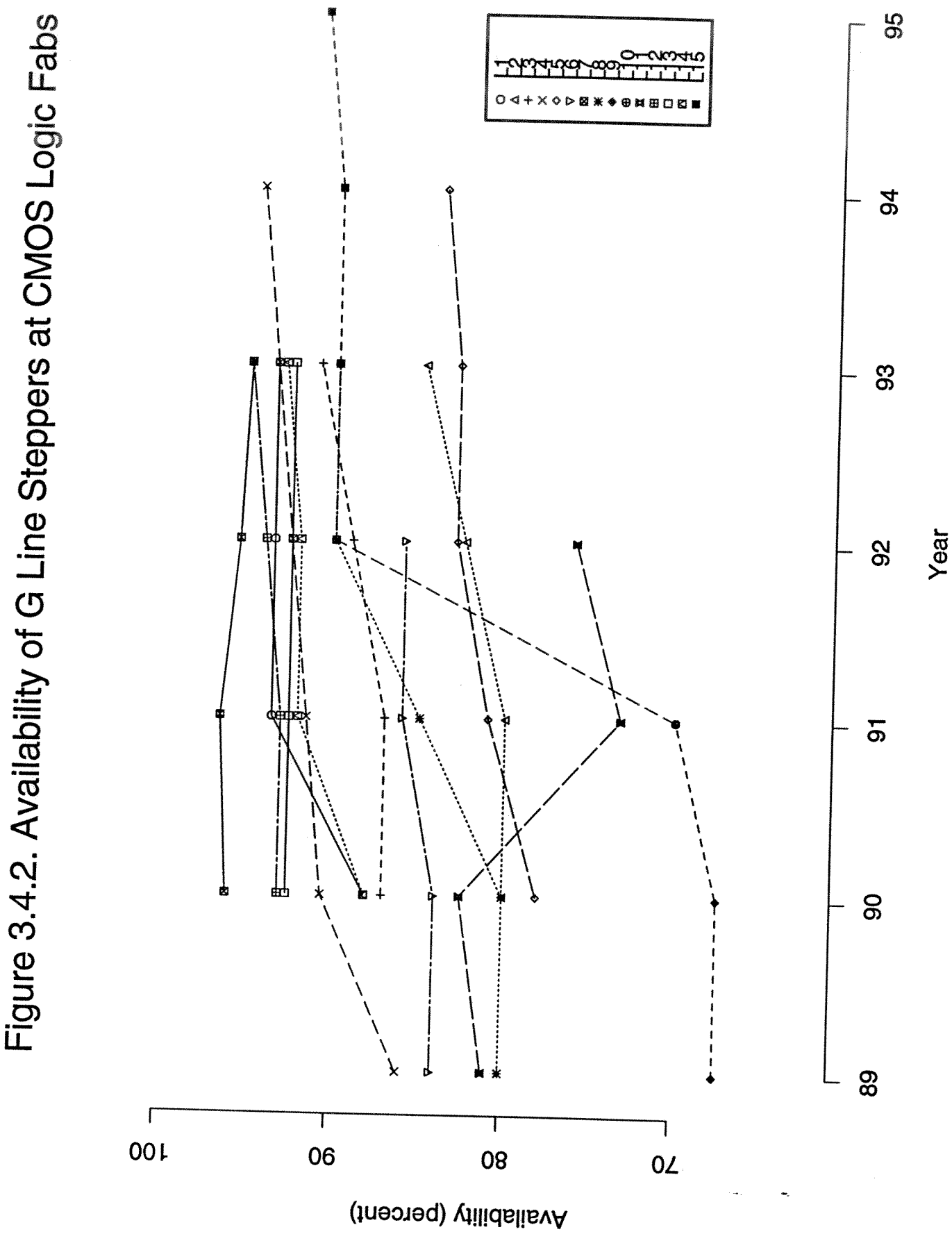


Figure 3.4.2. Availability of G Line Steppers at CMOS Logic Fabs
Availability (percent)
70
80
90
100
Year
89
90
91
92
93
94
95

Figure 3.4.3. Availability of G Line Steppers at MSI Fabs

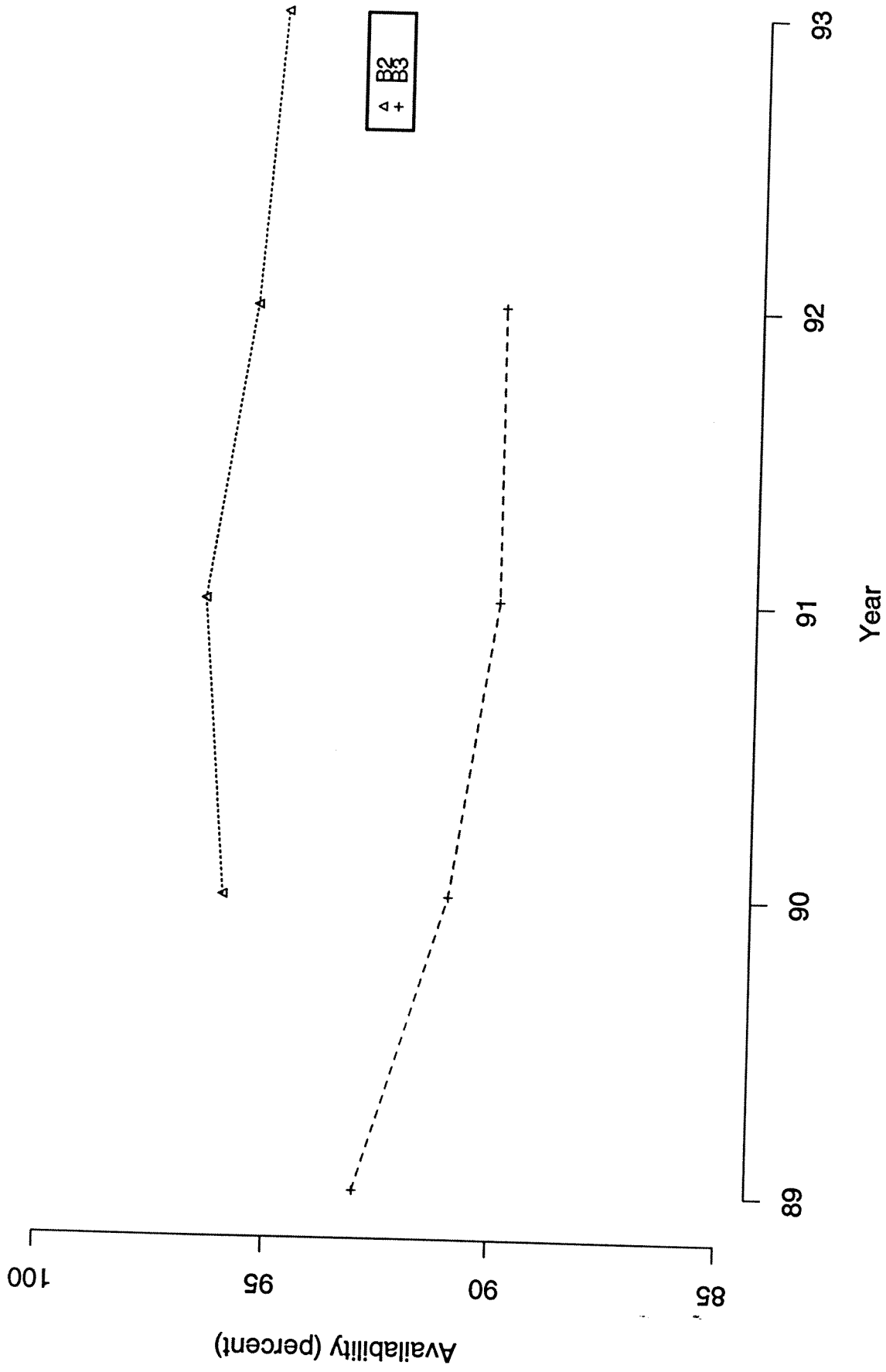


Figure 3.4.4. Availability of I Line Steppers at Memory Fabs

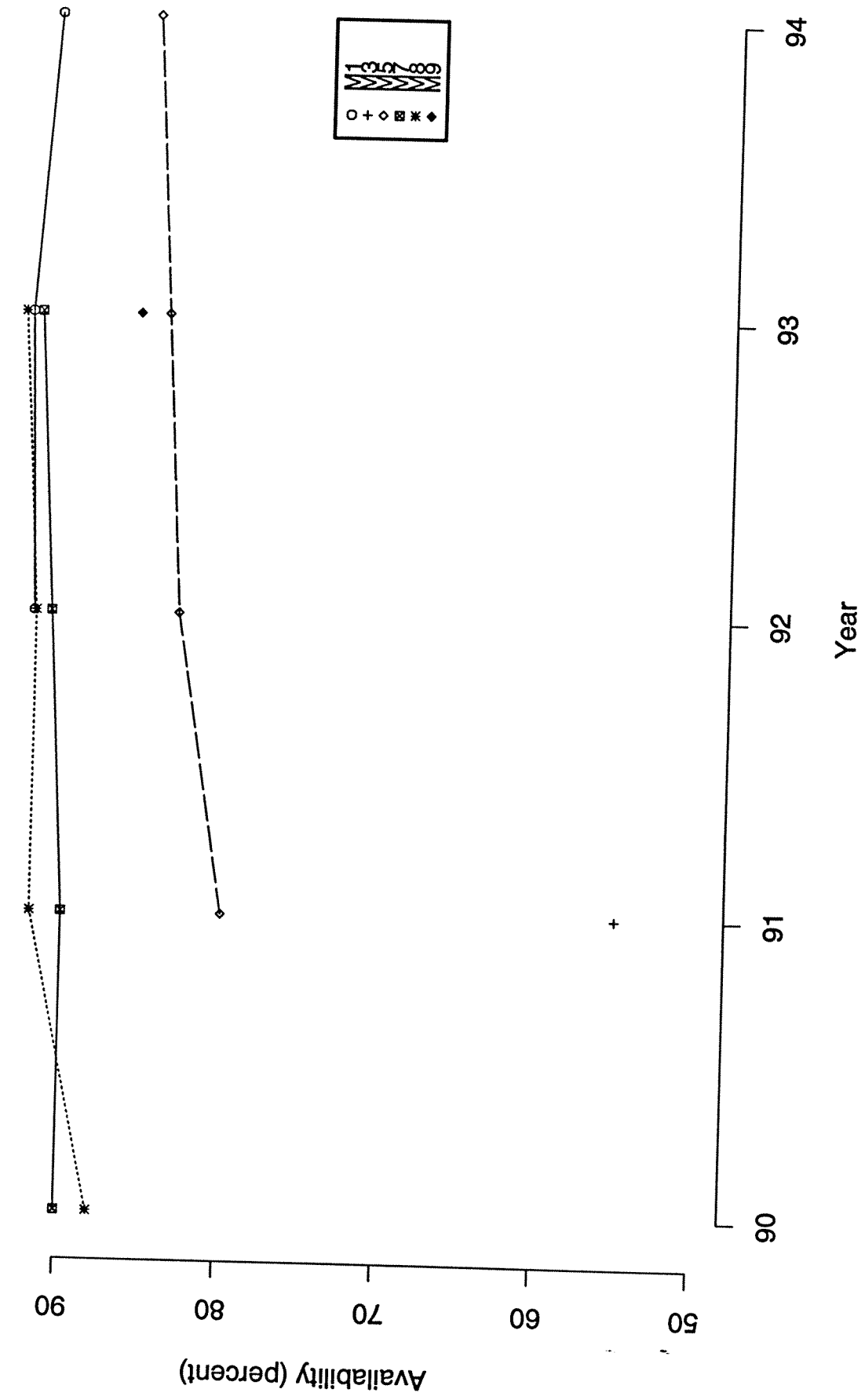


Figure 3.4.5. Availability of I Line Steppers at CMOS Logic Fabs

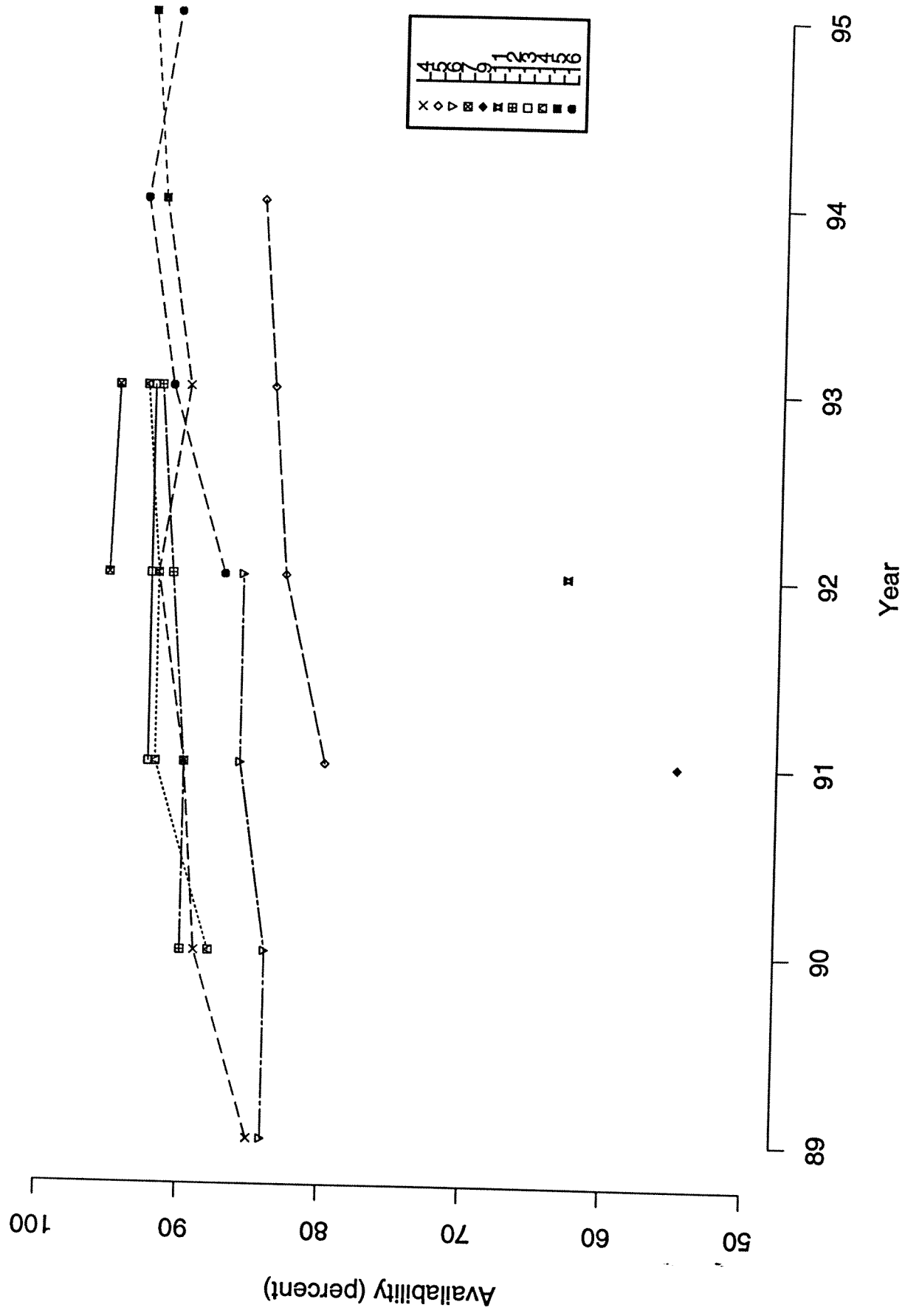
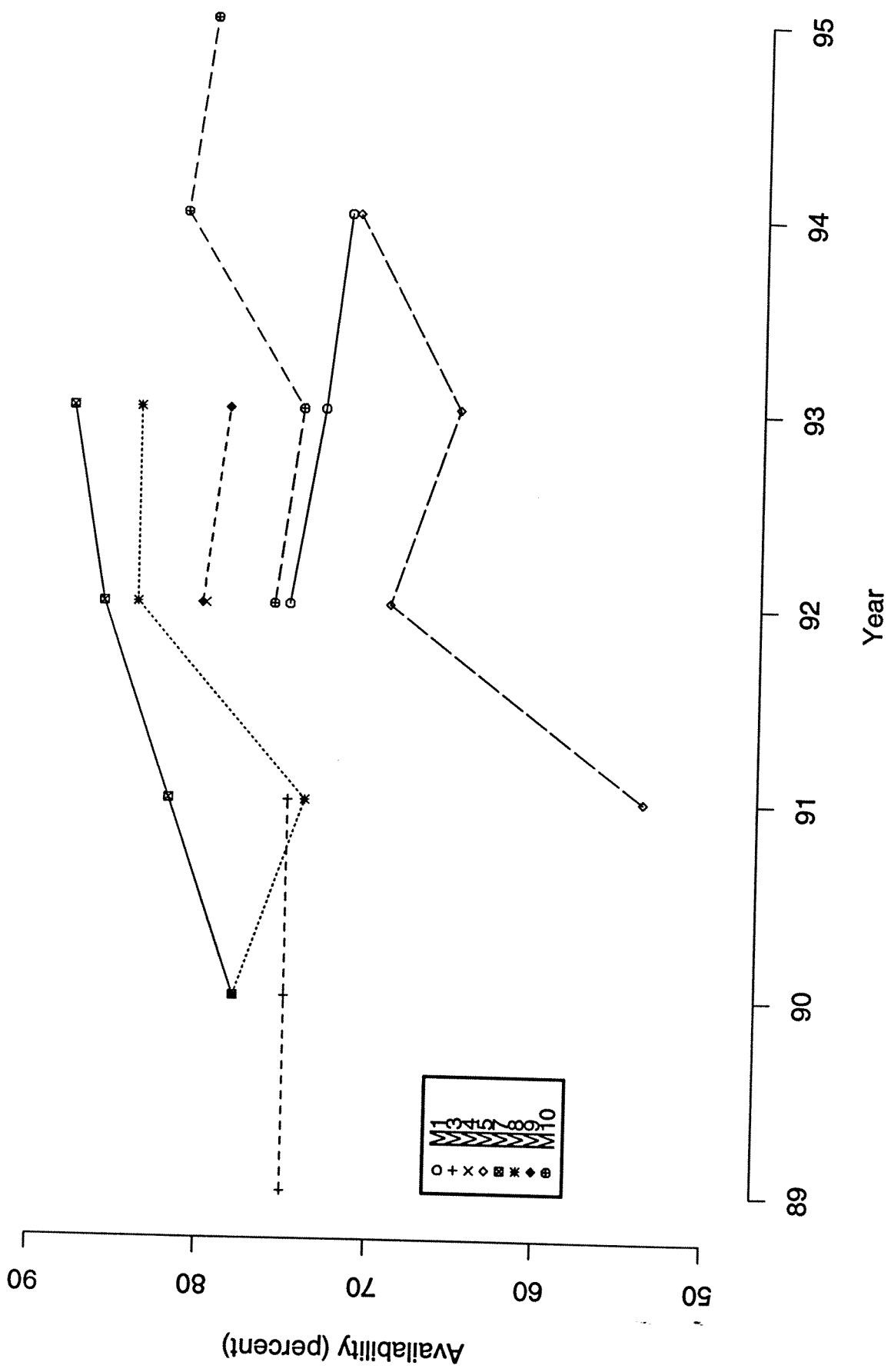


Figure 3.4.6. Availability of High Current Implanters at Memory Fabs



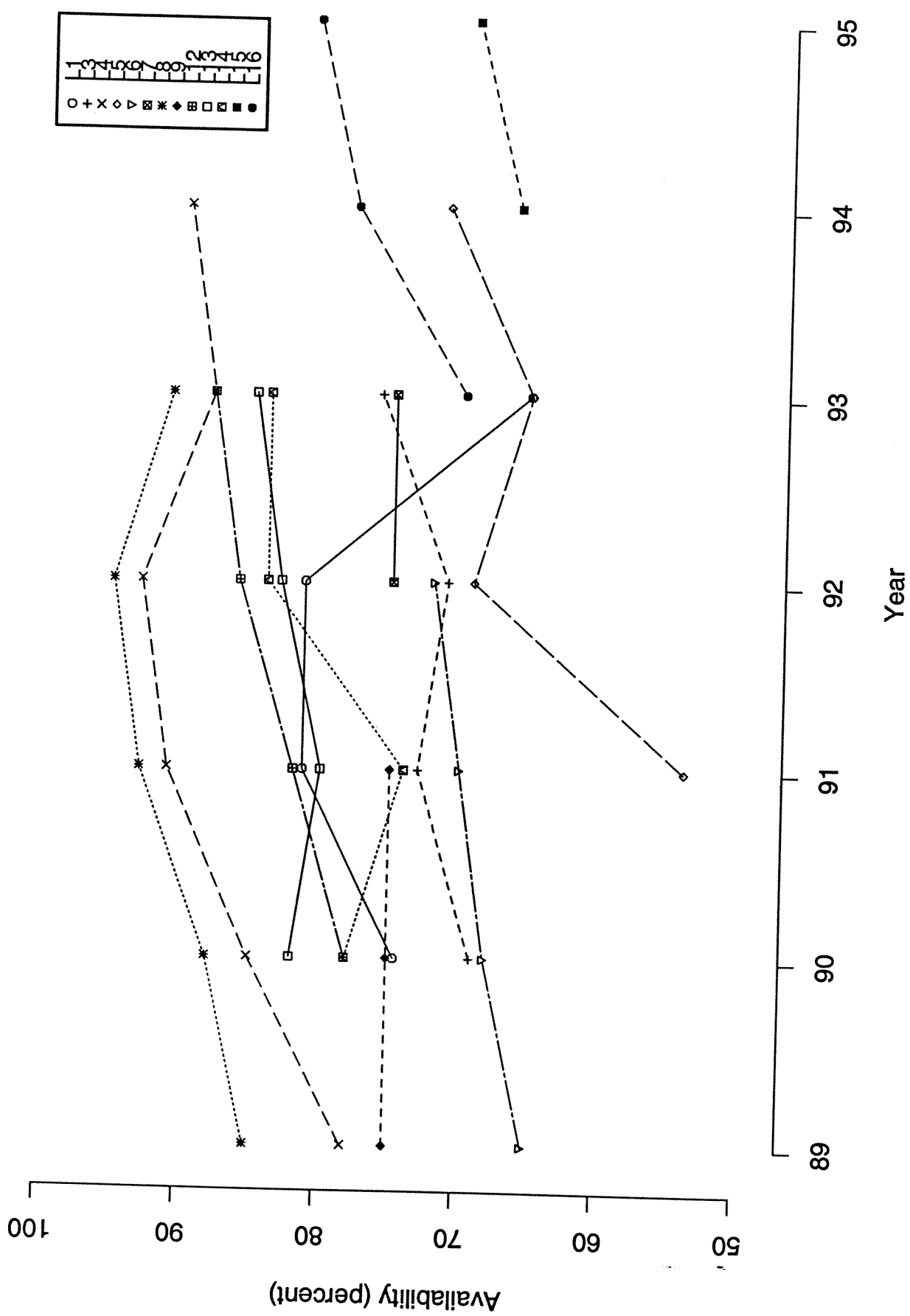


Figure 3.4.7. Availability of High Current Implanters at CMOS Logic Fabs

Figure 3.4.8. Availability of High Current Implanters at MSI Fabs

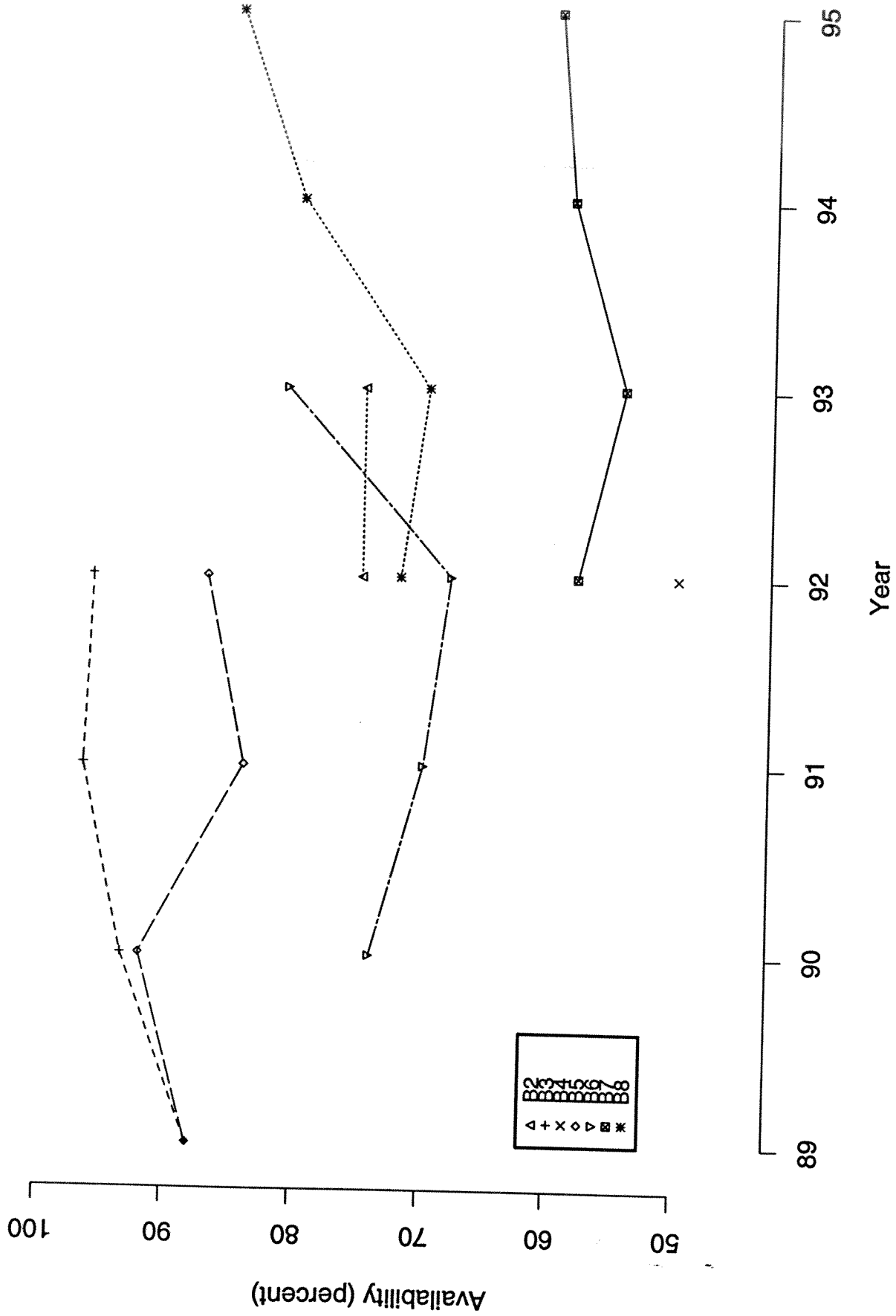


Figure 3.4.9. Availability of Medium Current Implanters at Memory Fabs

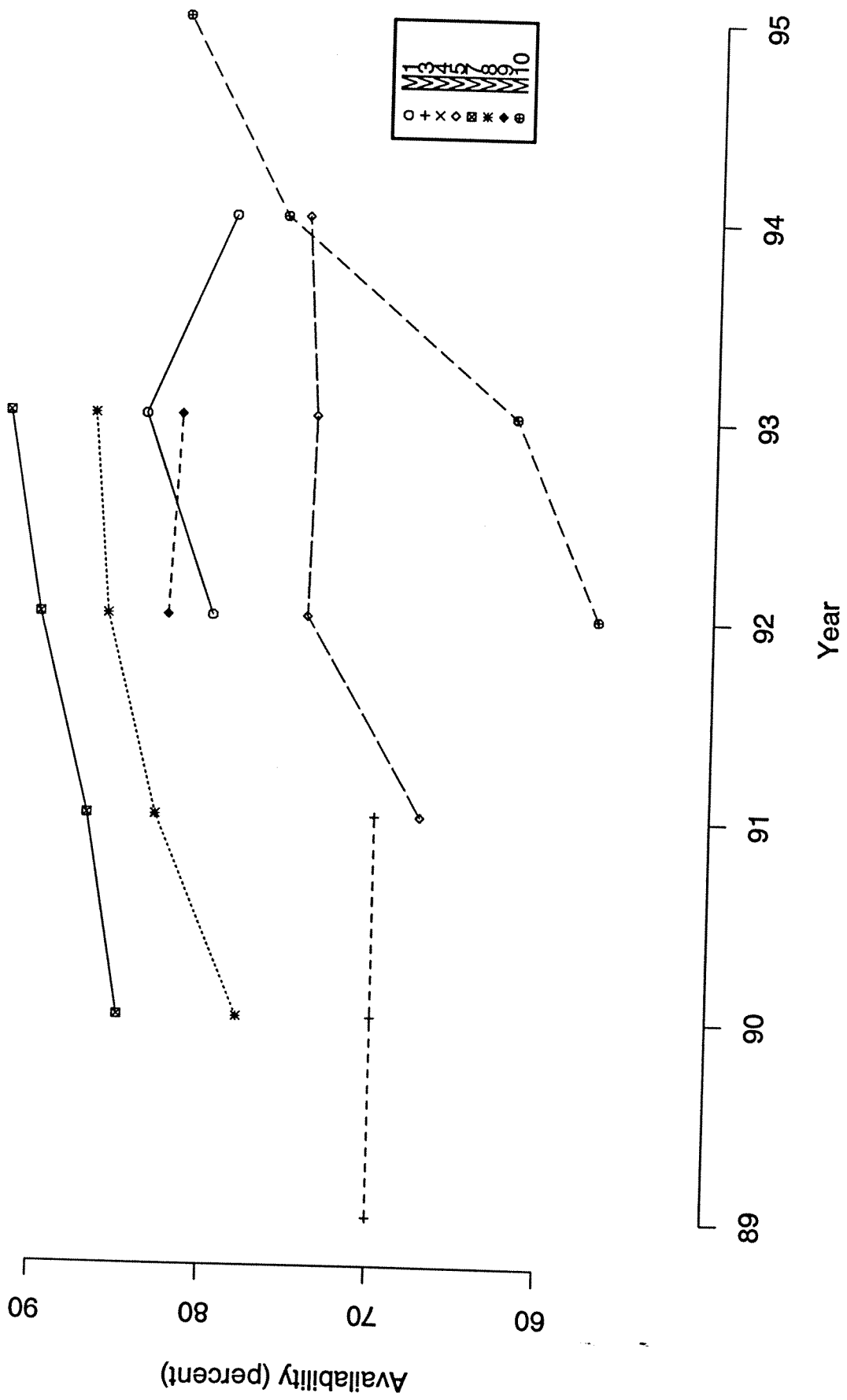


Figure 3.4.10. Availability of Medium Current Implanters at CMOS Logic Fabs

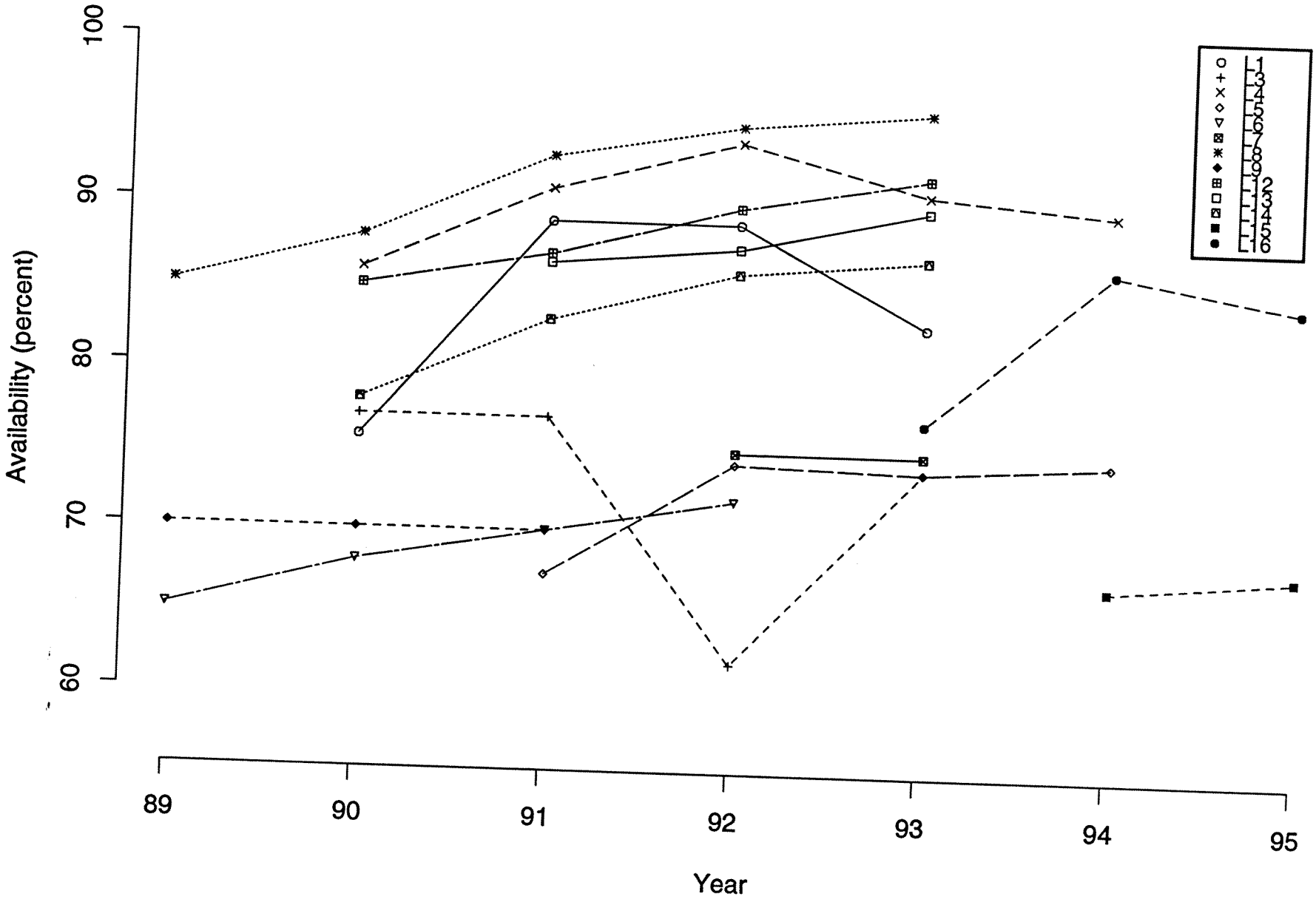
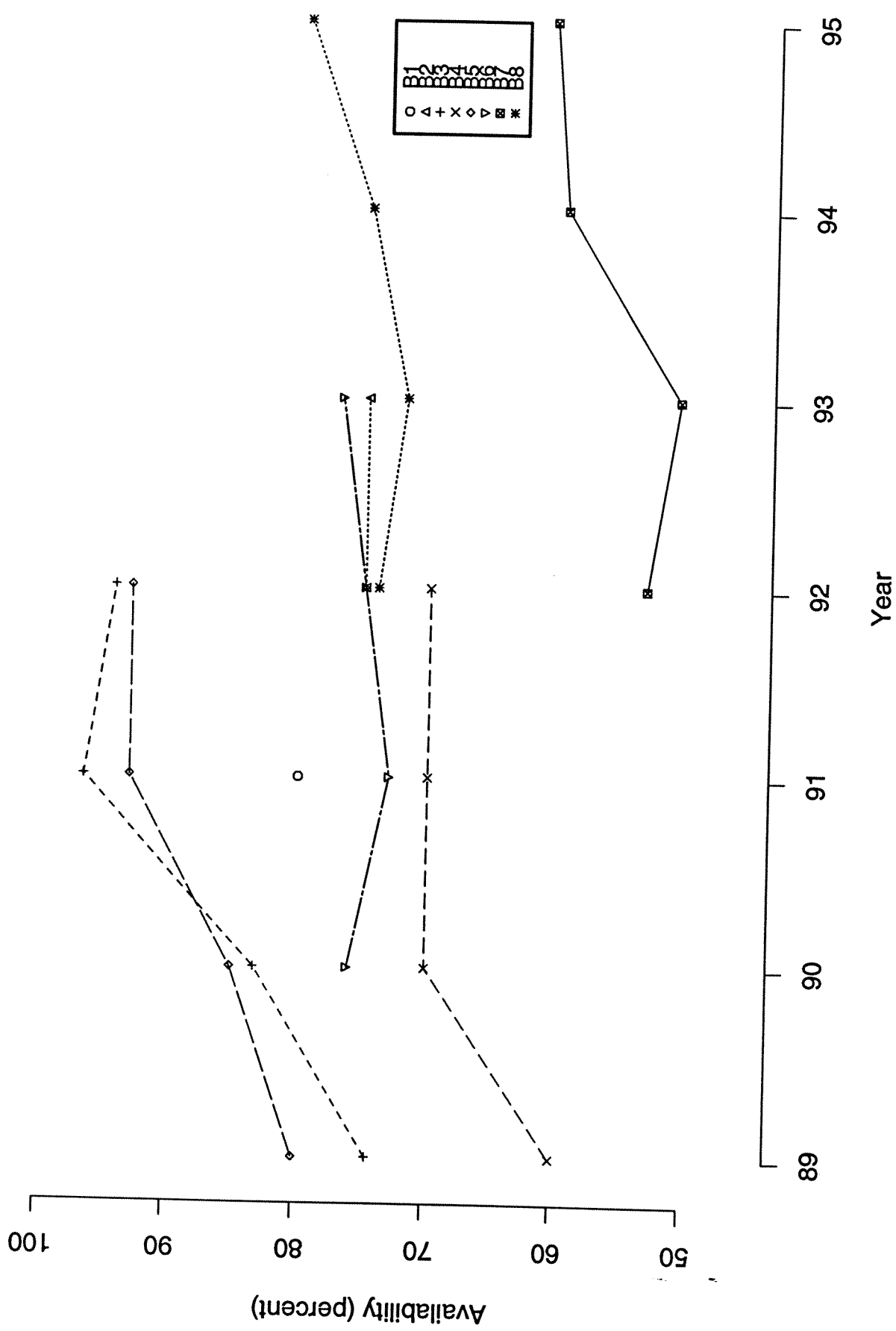


Figure 3.4.11. Availability of Medium Current Implanters at MSI Fabs



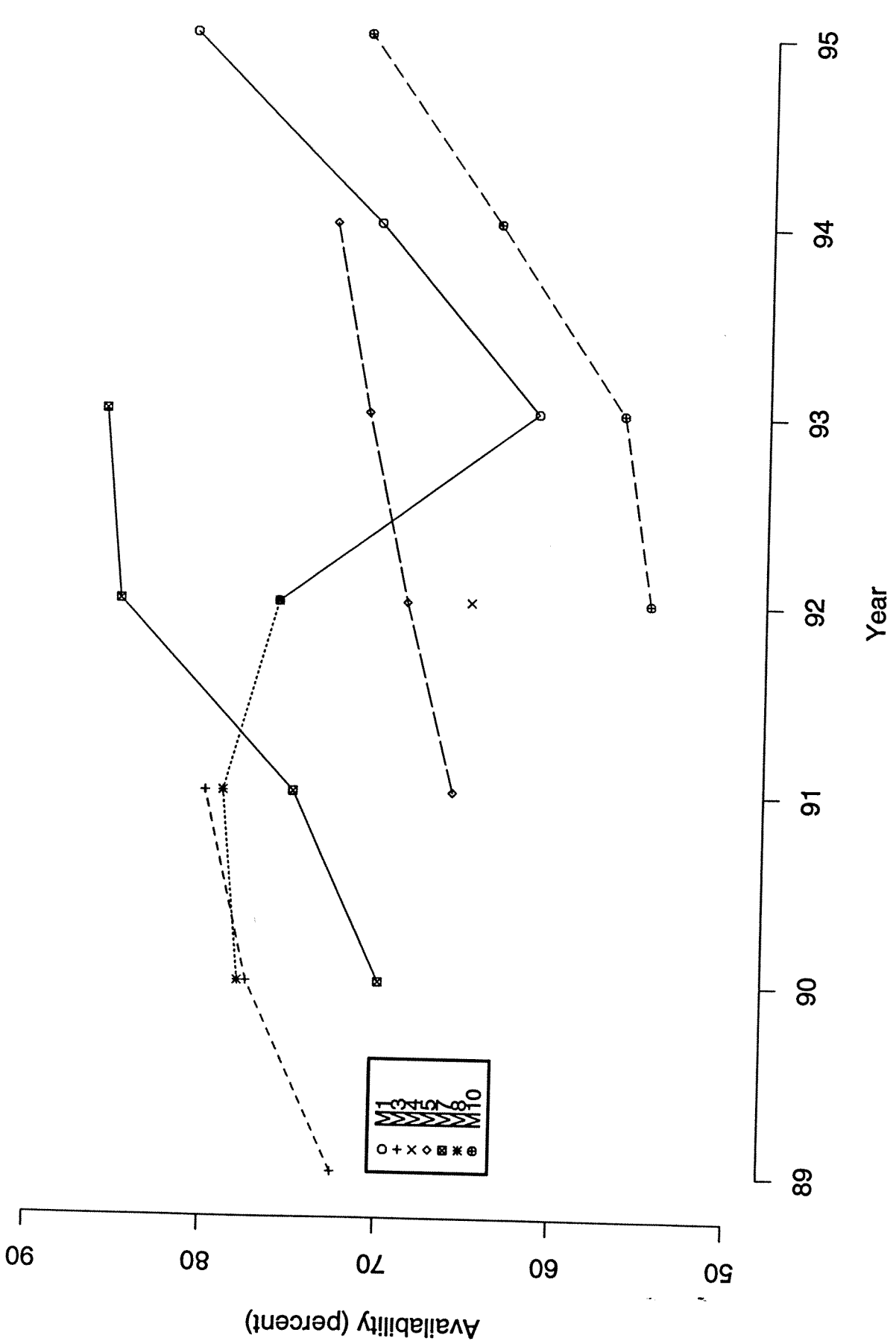


Figure 3.4.12. Availability of Metallization Machines at Memory Fabs

Figure 3.4.13. Availability of Metallization Machines at CMOS Logic Fabs

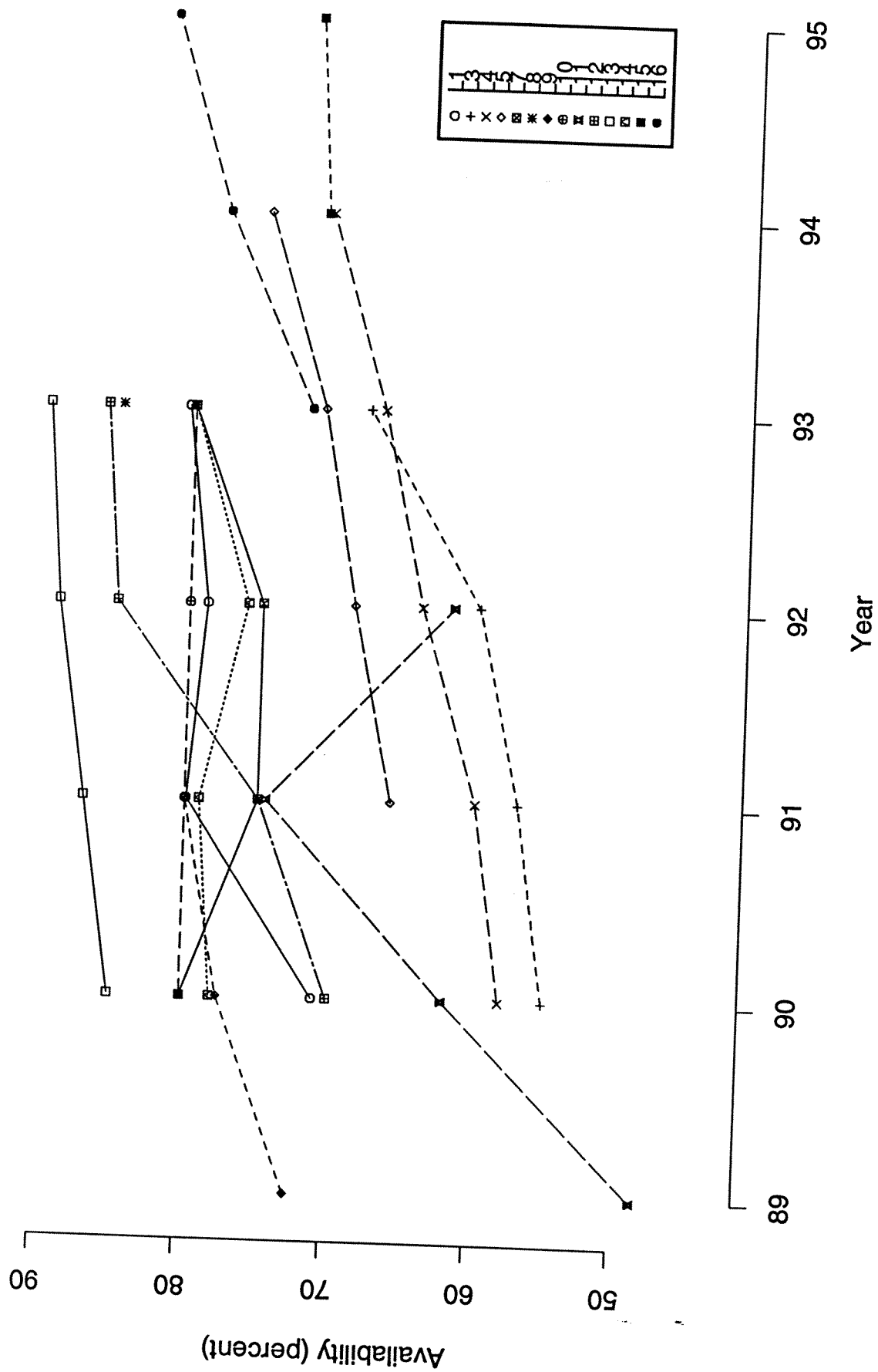


Figure 3.4.14. Availability of Metallization Machines at MSI Fabs

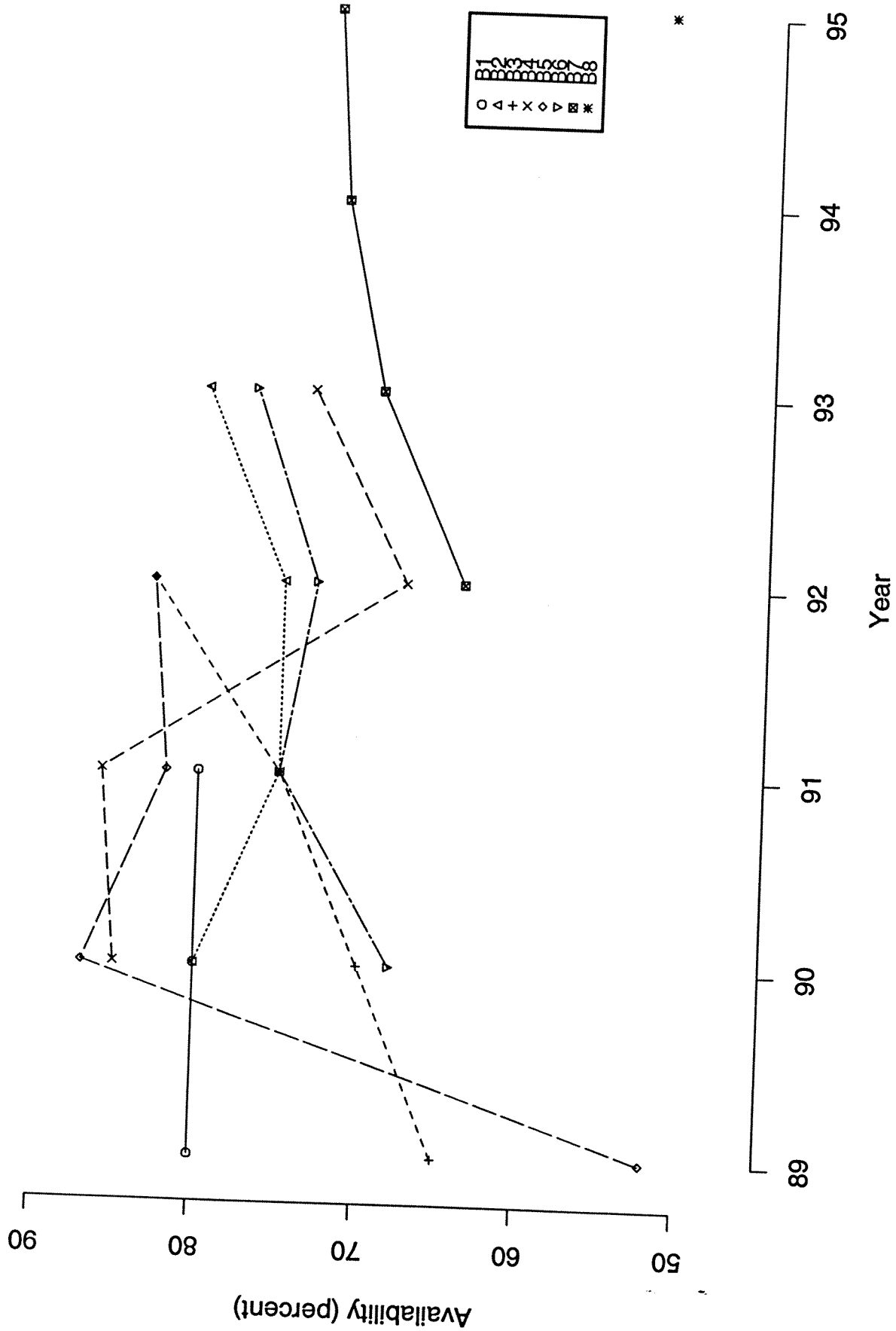


Figure 3.4.15. Memory Fab Technician Workload

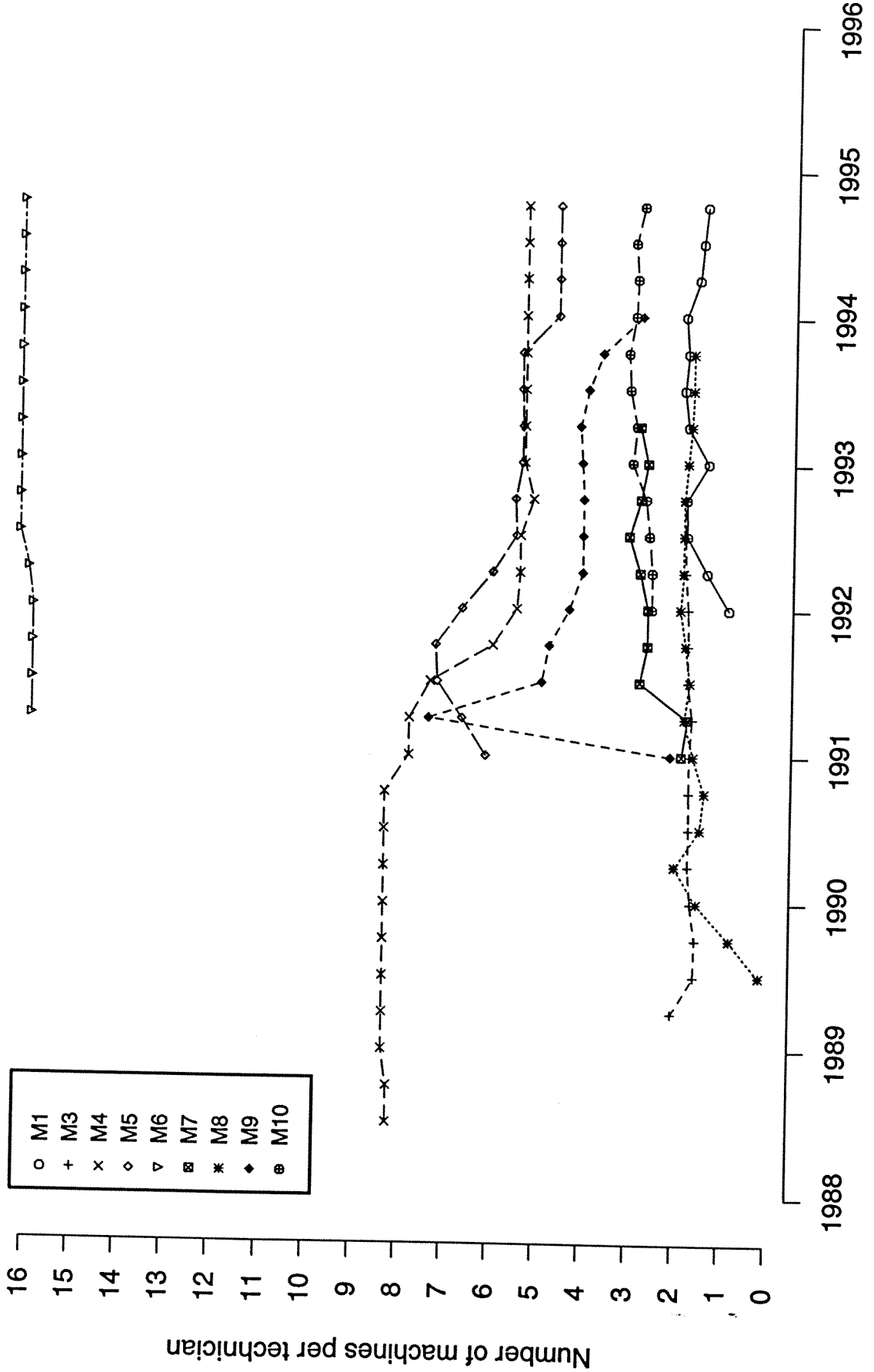
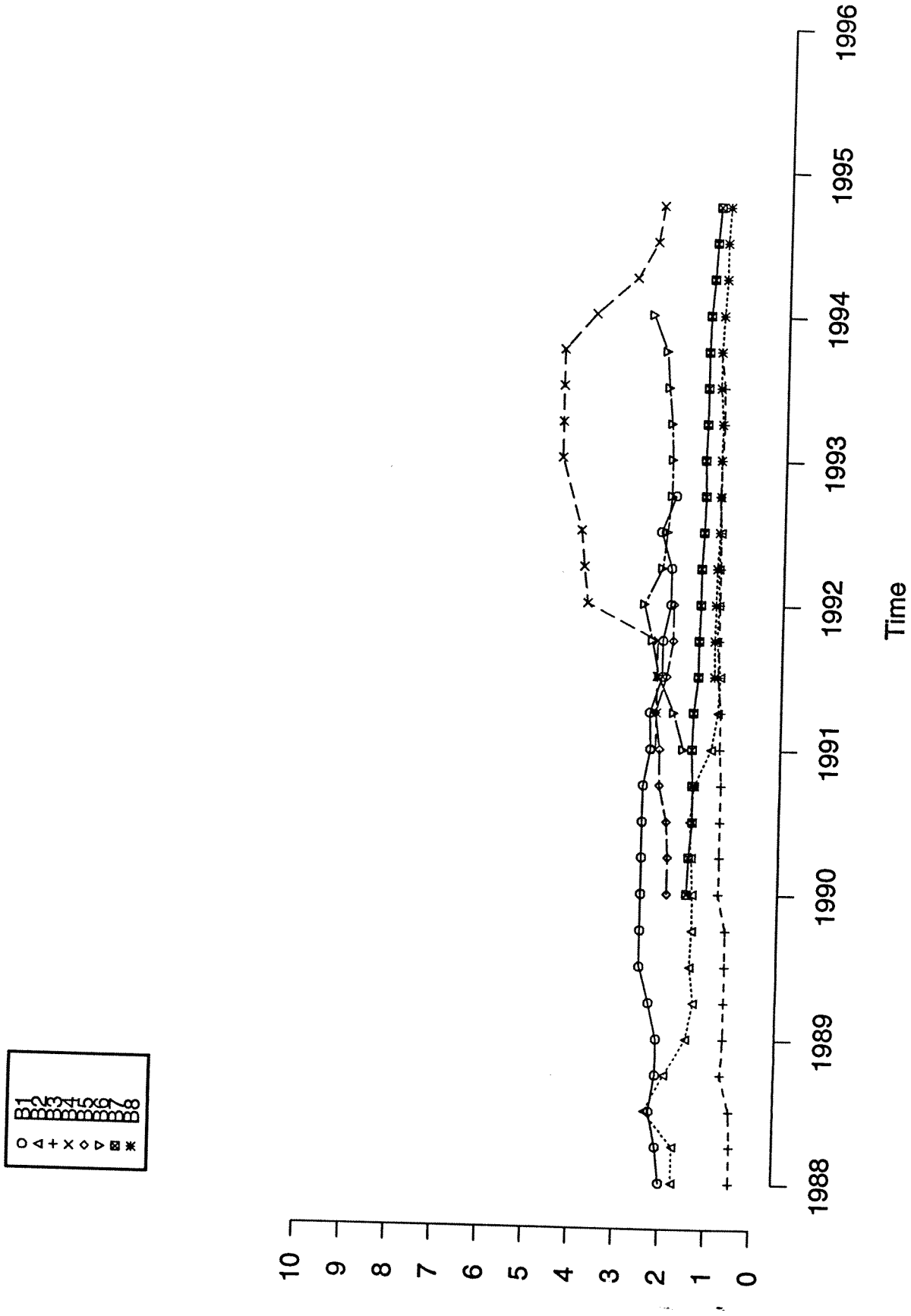


Figure 3.4.16. CMOS Logic Fab Technician Workload

Figure 3.4.17. MSI Fab Technician Workload



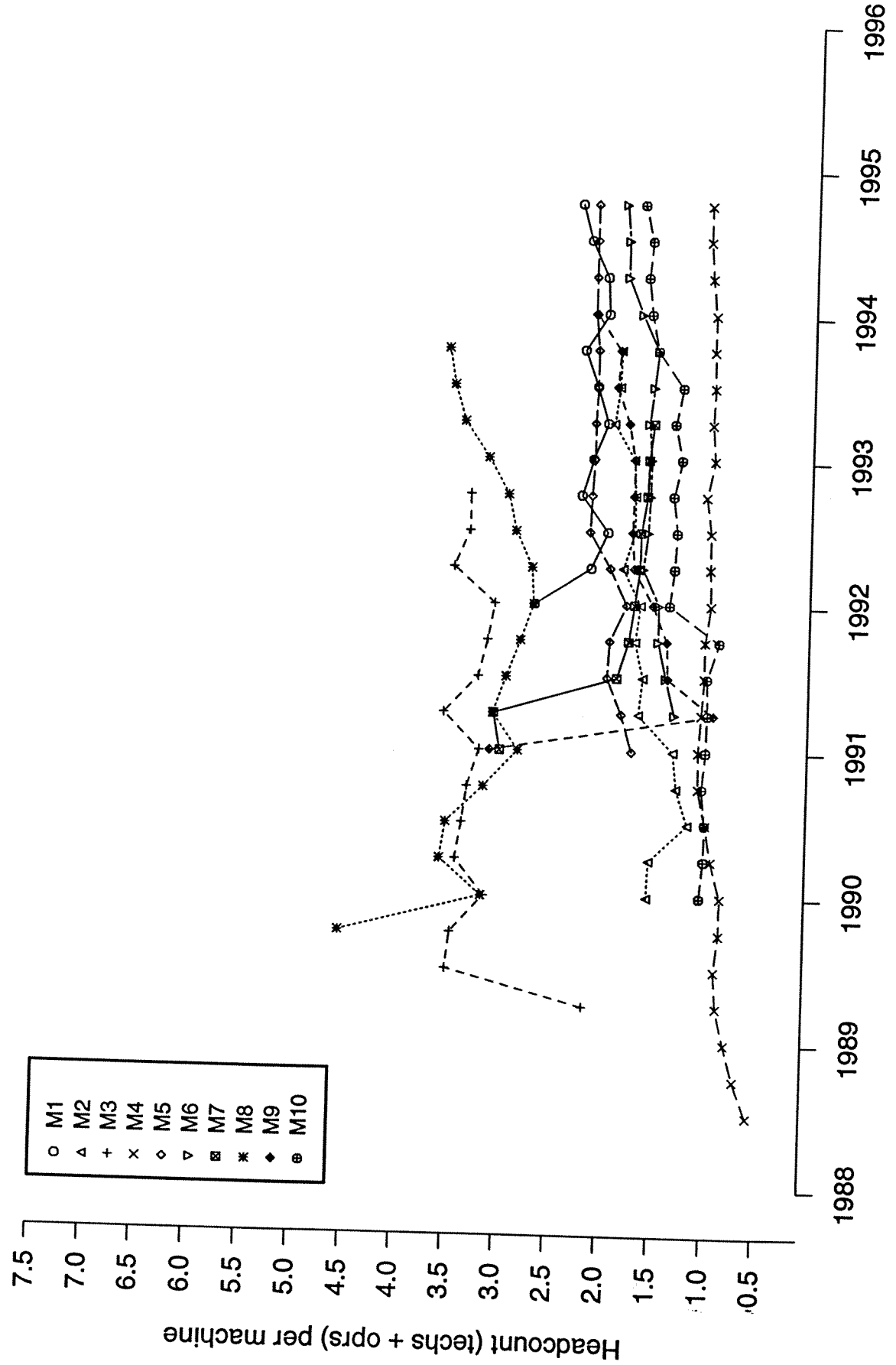


Figure 3.4.18. Memory Fab Headcount Per Processing Machine
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
Headcount (techs + oprs) per machine
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
1988
1989
1990
1991
1992
1993
1994
1995
1996
Time

Figure 3.4.19. CMOS Logic Fab Headcount Per Processing Machine

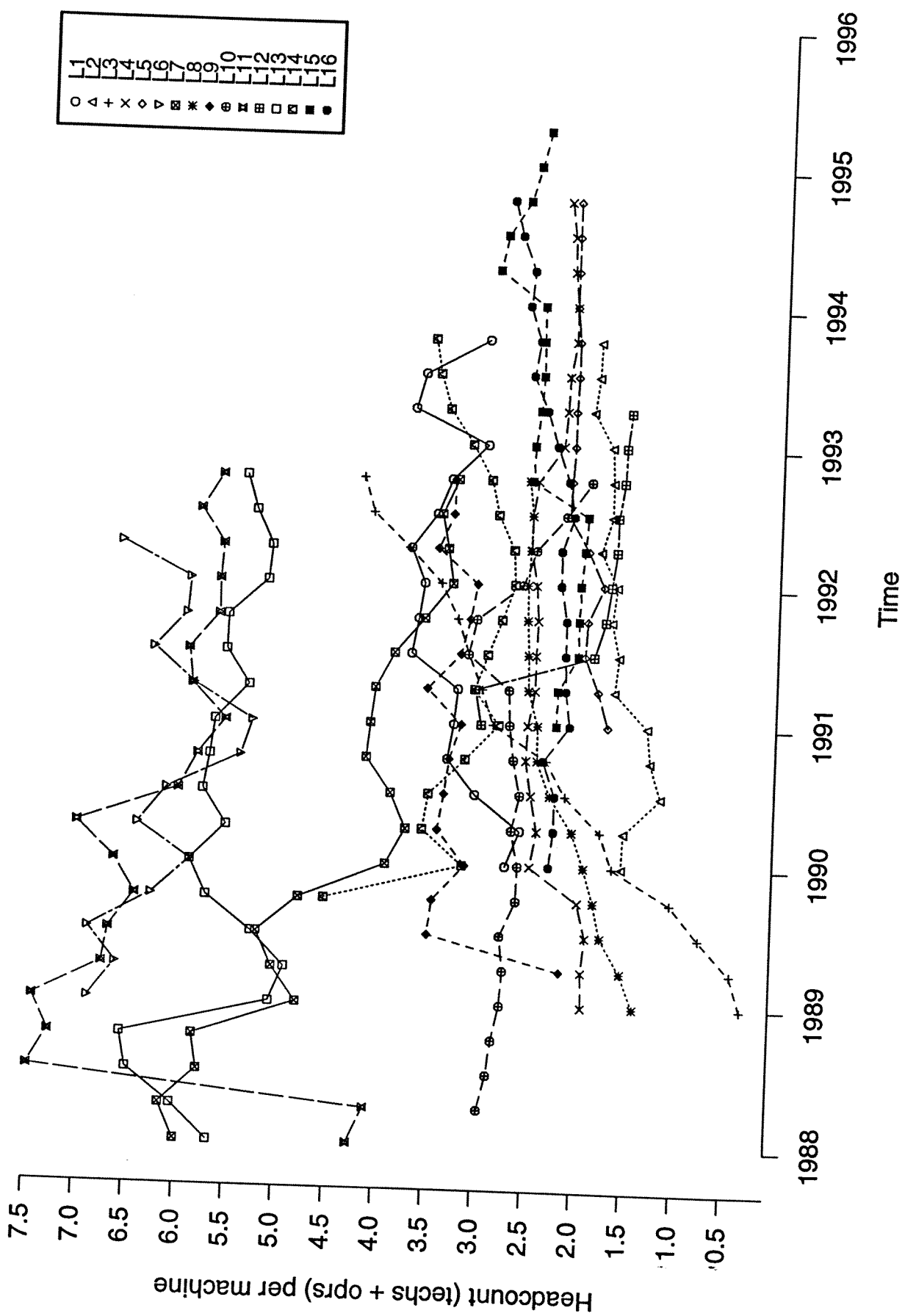
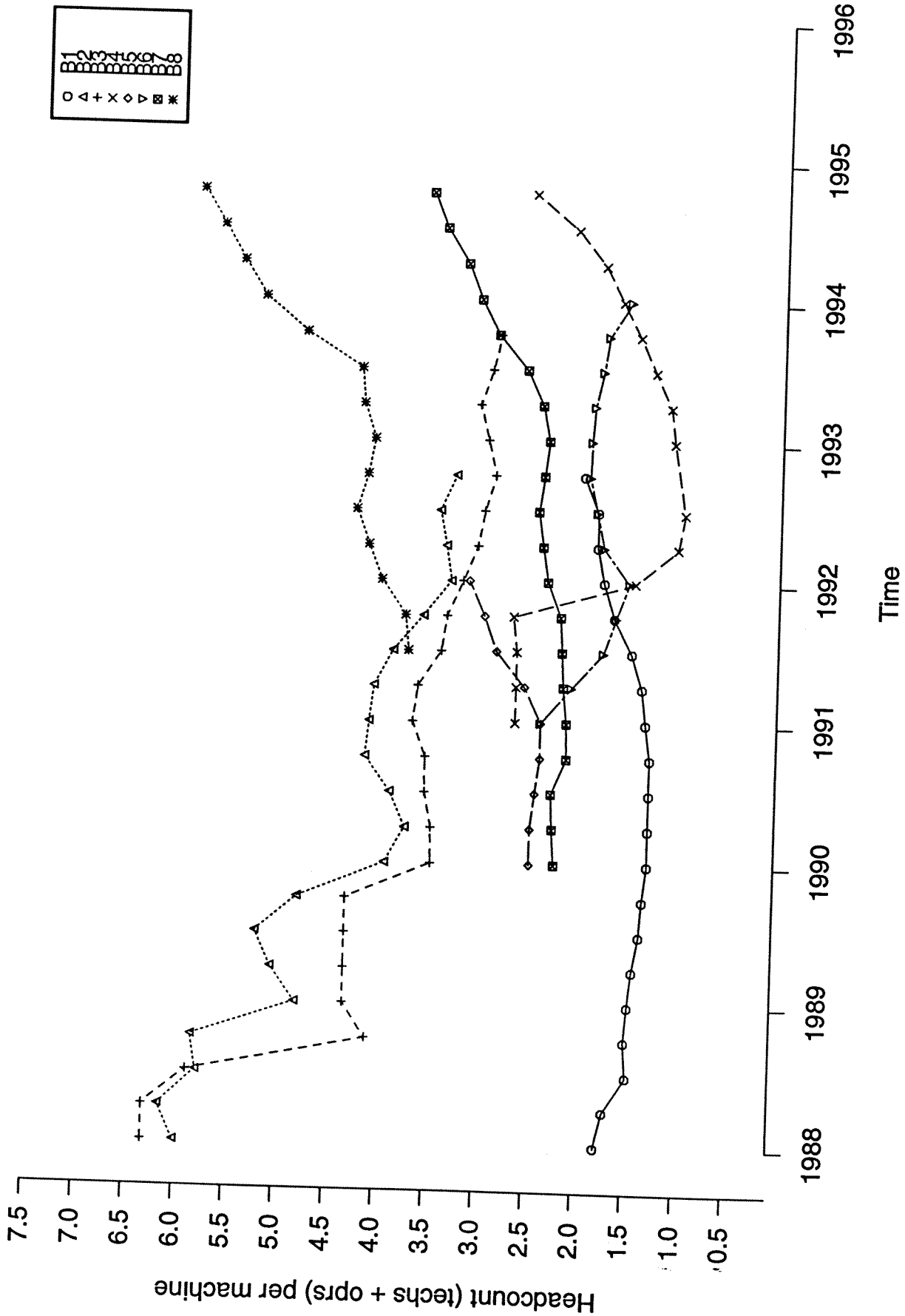


Figure 3.4.20. MSI Fab Headcount Per Processing Machine



3.5. Cycle Time Reduction
by Thomas Sloan

Cycle time, the length of time that it takes to manufacture a product, is an important performance metric in many manufacturing environments. Wafer fabrication consists of hundreds of steps in which a wafer travels a convoluted path through the fab covering a distance best measured in miles. Wafer processing is a complex manufacturing process in that a wafer repeatedly undergoes a series of interrelated steps performed on different types of equipment in order to build up multiple layers of circuitry.

The time spent manufacturing a wafer has two components: *value-added time* and *non-value-added time.* Value-added time is the time during which the wafer experiences a physical change through operations such as coat, expose, etch, etc. The non-value-added time includes the time spent by a wafer in transport, waiting for other wafers to be processed, and waiting for tests or setups to be completed. Large inventories of work-in-process (WIP) and long cycle times can result from unmatched speeds of the processing steps, unscheduled downtime of the machines, process problems, operator problems, etc. Many portions of the non-value-added component of cycle time can be reduced by better execution: reducing the frequency and duration of setups, reducing the number of test wafers, cross-training of operators, etc. On the other hand, reductions in the value-added component usually require significant physical changes: technology upgrades, process changes, equipment modifications, etc.

For semiconductor manufacturers, cycle time is an important metric for several reasons. First, it is an indicator of overall fab efficiency. Short cycle times suggest efficient fab layout and equipment configuration, reliable equipment with minimal downtime, effective production planning and scheduling, minimal equipment setup and changeover times, robust process design with minimal process tests, and a well-trained, reliable work force. Second, cycle time has a direct impact on responsiveness to customer demand -- an increasingly important competitive distinction in the semiconductor industry. For firms that produce to order, shorter cycle times reduce customer lead times, i.e., the time it takes for a customer to receive an order. For firms that produce to stock (or plan), shorter cycle times reduce the risk of forecast errors and excess inventories.

In our last report, [21] we concluded that cycle time is a function of many factors -- some that are within an individual fab's control and some that are not. In this report, we reconsider this conclusion and present a statistical model that sheds new light on the relationship between strategic decisions, fab-level practices, and cycle time performance.

Cycle Time Definition and Measurement

For our study, we shall define "cycle time" as the time interval in days from wafer lot release until the wafer lot processing is completed, including actual processing time, transfer time, and waiting time experienced by the lot. Since the fabs surveyed manufacture a different array of products requiring varying numbers of photolithographic layers, we do not compare total

21. See "Cycle Time Reduction," by Thomas Sloan, in *The Competitive Manufacturing Survey: Second Report on Results of the Main Phase,* R. C. Leachman (ed.), Report CSM-08, Engineering Systems Research Center, University of California, Berkeley, CA 94720 (September, 1994)

cycle time for process flows; instead, we compare "cycle time per layer" (CTPL). Several participating fabs include wafer probe in their definition of cycle time, but several of our participants do not have probe facilities on-site. Therefore, we have subtracted estimated probe times (and waiting times at probe) from those fabs that include probe in their cycle time measurements.

Many fabs express cycle time as a multiplier of "theoretical" cycle time -- the time it would take to process one lot in an empty fab (i.e., with no waiting time). While this is a useful measure to drive improvements within the fab, it is not helpful as an inter-fab comparison because definitions of theoretical cycle time vary widely. In addition, such comparisons would ignore reductions in theoretical cycle time achieved by improving equipment, redesigning processes, etc. Efforts to reduce theoretical cycle time seem to have a big impact on total cycle time (as discussed in greater detail below).

Many factors influence cycle time. Some of these factors are based on long-term, strategic decisions and remain fixed over long time horizons, e.g., process technology, market focus, etc. In general, individual fabs do not exercise a great deal of control over these factors. Other factors can be changed by relatively short-term, fab-level decisions, e.g., how to handle "rush" orders, cross-training of operators, etc. Below, we discuss some of these factors and share our observations about effective and ineffective practices.

Strategic Factors That Influence Cycle Time

We identify and briefly discuss below some of the strategic factors that influence cycle time and productivity improvement. By "strategic" we mean factors that are based on long-term technology and market choices that tend to be fixed over long time horizons. A firm's decision to produce 16 MB DRAMs, for example, is a high-level decision that affects (and is affected by) many other choices such as process technology, equipment, market, etc. Our hypothesis is that these choices will have a significant impact on a fab's cycle time performance. Many of the factors listed below will be included in the statistical model of cycle time performance presented later in this chapter.

Process/Product

(1) Number of mask layers: Clearly, more photolithographic mask layers will require more time to process, other things being equal. For this reason, we measure fab performance in terms of "cycle time per layer" (CTPL), as mentioned above.

(2) Technology type (bipolar or CMOS): CMOS processes generally require more mask layers and greater precision than bipolar processes, so we would expect longer cycle times for CMOS fabs. Focusing on the CTPL helps to minimize these differences.

(3) Wafer size: Larger wafers are desirable as they allow for more chips per wafer (i.e., economies of scale), but at some process steps they take longer to process than smaller wafers. Most fabs in our study produce five- or six-inch wafers, although several produce four-inch wafers.

(4) Process age: Other factors being equal, we would expect more-mature processes to have lower cycle times than less-mature processes. Although the impact on cycle time is not as dramatic as the impact on yield, it takes a great deal of effort to introduce new processes and "ramp up" to volume production. Ideally, process improvements, reductions in test runs, and

improved setups will lead to cycle time reductions as the process matures.

(5) Device type (memory or logic): Using the same basic equipment set, one can produce a variety of device types: memory, logic, microprocessors, etc. Although logic devices generally have high circuit densities, they are typically produced in a process technology one or more generations older than the technology used to produce current memory products. Therefore, we would expect logic producers to have shorter cycle times than memory producers.

(6) Minimum feature size: Smaller line widths generally require greater precision and, other factors being equal, may require more processing steps and perhaps longer processing time such as photo exposure time. Since photolithography is typically the long-run fab bottleneck, this may translate into higher cycle times.

(7) Die size: Like minimum feature size, the chip size can be an indicator of product generation. Traditionally, products go through several "shrinks," where circuits are squeezed into smaller spaces. This increases the precision required for the process and may result in more steps or more photo exposure time and hence, longer cycle time.

Facility/Equipment

(1) Clean room size: Large fabs are capable of great economies of scale, but the physical size of the clean room can also have negative effects on cycle time and productivity. We have visited several large fabs where operators must travel long distances to (for example) retrieve reticles. Large fabs may also inhibit communication between operators in different areas. Efficient layout, automation, and improved information systems (discussed below in a sub-section on practices) are several strategies that firms use to overcome these obstacles.

(2) Equipment age: In general, newer machines are capable of higher precision than older machines and may require less processing time for a given product type. Process technology changes can have a big impact on cycle time. For example, several fabs have reduced processing time and improved yield by employing ion implanters instead of diffusion furnaces. On the other hand, equipment using cutting-edge technology may be more susceptible to breakdowns as the equipment is not fully-characterized.

(3) Equipment efficiency: Equipment efficiency refers to the proportion of time that a machine is engaged in production, adding value to the product. This metric is particularly important for the bottleneck resource as it directly affects total fab throughput. Idleness at the bottleneck resource is lost time that can never be recovered. (For further discussion, refer to Section 3.4, Equipment Efficiency Improvement.)

Market/Volume

(1) Customization (commodity or ASIC): It is much more difficult to forecast demand, and hence plan production, for custom products (so-called application specific integrated circuits, or ASICs). In general, ASIC producers have a stronger incentive to reduce cycle time as it directly affects their customers. Fabs that mainly produce commodity products can maintain an inventory of finished goods. However, this reduces their ability to respond to shifts in demand and technological innovations.

(2) Customer (captive or merchant): Some fabs are captive in the sense that they only produce devices for use by their parent companies (e.g., IBM, DEC, and AT&T). In theory, this should

make demand forecasts easier as they should have a better idea of the "true" demand for the product. In practice, however, captive fabs sometimes experience bigger demand shocks than merchant fabs. For example, financial problems of the parent company may force new product lines to be curtailed, reducing the demand for the components supplied by the fab. One participant reported that the product lines that they serve can cancel orders up to one day before the product is due without incurring a penalty.

(3) Capacity utilization: The capacity of the fab is restricted by the bottleneck resource, usually photolithography. When the fab is running close to capacity, any disruptions -- machine downtime, yield crashes, demand changes -- can have a dramatic impact on cycle time. Other factors being equal, a fab with lower capacity utilization will have shorter cycle times than a fab with higher capacity utilization.

(4) Number of process flows: Fabs can produce several different device types (e.g., memory and logic) using the same equipment set. More processes add complexity to the manufacturing process, as one must contend with more recipes, demand variations, etc. The introduction of new processes can be particularly disruptive.

(5) Number of products: Many different die types can be produced from a single process flow, and this adds complexity to the process, especially at the photolithography step. Increasing the number of products increases the number of machine setups, reticles, and recipes and can increase demand variability.

Fab-Level Improvement Practices

We now identify and discuss briefly the fab-level practices that we believe are associated with cycle time performance. These practices involve operational decisions that are more flexible than the strategic decisions discussed above. For example, the number of test wafers that a fab processes today does not depend on the number it processed last week. The practices we identify can be divided into four broad categories: production control, automation, process/equipment, and communication/information systems. A discussion of each category follows.

Production Control

Top performers have developed effective systems to regulate wafer starts and monitor and control the flow of WIP. Sometimes the most effective systems are the simplest. Some production control practices that we observed include:

(1) Production planning system: Top performers have implemented effective production planning systems that help regulate starts to meet demand and keep the bottleneck resource fully loaded without excessive WIP. This requires accurate demand forecasts, awareness of capacity constraints, and predictable performance parameters such as yield and cycle time. (For further discussion of production planning systems, refer to Section 3.7, On-Time Delivery.)

(2) Shop-floor control system: Top performers have systems to monitor and control WIP flow and buildup within the fab. Kanban systems seem to be popular, and several top performers use them. However, several mid- to low-performers also use Kanban systems, so the details of the control methodology would seem to be important.

The fab with the shortest CTPL in our survey establishes Kanban limits between major steps in each process flow. Large, ceiling-suspended color video monitors throughout the fab

display tables with an ingenious color coding scheme that allows operators to check at a glance Kanban status, schedule status, machine status, and to identify problem areas within the fab. The monitors display a table with columns for each process flow and rows for each major process step. A cell of the table representing a major process step in a particular flow is colored red if under a Kanban block, yellow if there is one more lot to go before a Kanban block occurs, and green otherwise. The cell is flashing if the process step is behind schedule (in terms of number of lots that should be completed by now). Small codes in the corner of the cell indicate how many machines that perform the process step are currently down. Thus, an operator can immediately grasp which operations should be performed from a schedule point of view, which should not be performed from WIP/Kanban point of view, and why some process steps are having trouble.

One fab we visited uses a "least slack" lot dispatch rule in which a lot's priority increases as its elapsed cycle time increases. This greatly reduces the variance of cycle times (thereby greatly improving on-time delivery), but it also seems to have a positive impact on average cycle time as well. This fab achieves good CTPL scores, but what is most striking is that the difference between the mean cycle time and the "one hundredth percentile" of cycle time (i.e., the cycle time of the worst-performing lot during an observation period) for 9-layer process flows is only two days! This remarkable performance gives this fab a substantial service advantage for cycle-time-sensitive products such as ASICs.

(3) Hot lots: Almost all fabs have high priority lots that receive special treatment. These lots may be special orders by customers, new process test lots, or simply lots that have fallen behind schedule. Although these lots generally have lower-than-average cycle times, the additional set-ups needed and waiting time caused by these lots may cause a net increase in mean cycle time. As long as the number of hot lots (as a percentage of WIP) is relatively small, the impact on cycle time will not be significant. It is interesting to note that the fab with the lowest CTPL does not have any hot lots. Their cycle time is so low that, in effect, every lot receives hot lot service.

(4) Holds: It is not uncommon for lots to be put on hold due to processing malfunctions until an engineer can test the lot. The number of lots on hold does not seem to be as important as the duration of the hold. In some poor- performing fabs, engineering holds are not included in the calculation of cycle time and are not tracked by the production control system. This makes it difficult to determine actual load levels at the various work stations.

(5) Engineering test lots: All fabs process engineering lots that are used for yield improvement tests, new product development, new process development, etc. These lots are certainly important for learning and improving performance, but their treatment can have a significant impact on production lots since they are competing for the same scarce resources. Some poor performers did not include engineering lots in their cycle time measurements and did not track them with the production control system. As with the hold lots, this makes it difficult to determine actual load levels at each work station.

Automation

IC manufacturing is a complex process involving a series of interrelated steps which are repeated over and over. Automation of certain functions can help reduce overall cycle time. (These issues are discussed in more detail in Section 3.6, CIM and Automation.)

(1) Linking of photo equipment: Several fabs have improved the efficiency of the photolithography operation through robotic or track integration of the stepper and aligner exposure machines with coat and develop tracks. Linked photo cells dramatically reduce the cycle time required to pass lots through photolithography operations. Since photolithography process steps are more frequent than any other kind of major process step, there is high leverage on cycle time associated with the introduction of such technology. Several high-performing fabs -- including five out of the top ten -- have linked photo cells.

(2) Material handling: In most fabs, operators hand-carry lots between operations within a particular operating area (e.g., diffusion). Carts are used to transport lots between different processing areas. Several fabs use automatic guided vehicles (AGVs), and several others have an overhead monorail system. While such systems seem to have a positive effect on cycle time in large fabs, they would probably be impractical for smaller fabs and would not significantly reduce cycle times.

(3) Automatic recipe download: In most fabs, operators must manually adjust machine settings for particular lots or sets of lots. This can be time-consuming, and a lot can be ruined if the wrong "recipe" is used for a particular process step. Some fabs have overcome this obstacle by storing recipes for individual lots (by product type) in a computer database. These recipes are automatically downloaded to machines when the lots are logged in at that station. This type of system can also be used to ensure that lots are processed in the proper sequence. For example, the machine will refuse to accept a lot that has not completed the appropriate upstream process step.

Moreover, the introduction of automated recipe download may reduce the need for test runs before processing the lot. For example, it may be feasible to reduce the frequency of test runs from once before every processing cycle (or every setup of a new process step) to once every shift. Elimination of test or pilot runs has a very substantial positive effect on cycle times.

(4) Wafer load/unload: The use of robots and handling mechanisms for load/unload tasks seems to have a positive effect on cycle time. In addition to the linked photo cells discussed above, a number of participants have introduced robotics for load/unload of diffusion, metalization, and wet bench operations. Two of our participants make extensive use of SMIF (standard mechanical interface) technology. Varying amounts of software and hardware controls governing lot load/unload can be installed along with SMIF. One fab making minimal investments in this regard claimed that cycle time went up as a result of introducing SMIF. The other utilizes extensive software and controls to assist lot and reticle retrieval, to automate reticle setups at photolithography, to check that the lot has been placed on the correct machine, to automatically download recipes into machines, and to automatically update WIP and equipment tracking records. This fab feels their SMIF program reduces time spent loading and unloading equipment, entering data, and retrieving lots and reticles, thereby making a very positive impact on cycle times.

(5) Automated data entry: All of the fabs in our study have computerized lot- tracking systems, some integrated with lot dispatching and process control systems. At most fabs, operators manually enter the data on computer terminals located near each work station. Some fabs record data using bar codes, and a few fabs use magnetic cards that travel with each lot to record appropriate data. Several fabs have abandoned bar codes in favor of manual entry. The method of data entry did not seem to have an impact on overall cycle time. In fact, data entry at the fab with the

lowest CTPL is performed via manual keyboard entry.

Process/Equipment

Above we discussed process and equipment as technological variables that influence cycle time. However, given a particular equipment set, many practices will affect cycle time performance. Some of these include:

(1) Equipment layout: The vast majority of our participants use a "farm layout" in which all machines of a particular type are located in the same equipment bay. Several top performers have abandoned this in favor a more cell-based layout featuring a set of dissimilar machines performing a series of operations. Many fabs have been forced to rearrange equipment as new machines are added and new processes are introduced. However, the top performers seem to be willing to make major changes for the sake of improving efficiency, and the impressive cycle time performance by these fabs suggests that their efforts have paid off.

(2) Re-design of process/equipment: In some cases, it is possible to reduce cycle time by making process changes. The top performer with respect to cycle time was able to replace long diffusion steps with much quicker implant steps. One intermediate performer was able to eliminate many steps from the process flow including two entire mask layers. Some improvements were of a much simpler nature. For example, one high performer had problems cleaning a particular machine. By modifying the equipment, they were able to reduce the setup time and improve the maintainability of the equipment. We heard similar stories from many of our participants.

(3) Quality control practices: Yield is a critical performance metric in semiconductor manufacturing, and most fabs that we have visited have implemented quality control systems, including statistical process control (SPC) and wafer inspections, to help improve yield. However, some fabs run so many quality checks and engage in so much analysis that there seems to be a net loss in productivity. Carefully measuring cycle time performance can reveal such productivity losses.

Several fabs have made great efforts to "mistake proof" processes through simplification, automation, "buddy checks," etc. In some cases, these efforts can lead to reduced efficiency. For example, many steppers are equipped with compartments to store several reticles. There is great potential to reduce machine setup time (and hence cycle time) by keeping reticles that will be needed during the shift close at-hand. However, several fabs failed to take advantage of this opportunity because they felt that the risk of using the wrong reticle outweighed the potential productivity gains.

This helps explain the wide disparity in setup times in different fabs for the same equipment type; in one fab, a stepper setup takes 30 minutes and in another fab, a stepper setup takes only two to three minutes.

(4) Equipment maintenance: Preventive maintenance programs have proven to be a valuable tool in reducing equipment failures and misprocessing. Such efforts to reduce variability and maintain proper machine performance speeds tend to have a positive effect on cycle time performance as well. (For more discussion on this subject, see Section 3.4, Equipment Efficiency Improvement.)

Communication/Information systems

Section 3.6 (CIM and Automation) in this report discusses the impact of information technology -- how data are collected -- on fab performance. Below we discuss how the data are used and the impact of these practices on cycle time performance.

(1) Communication with line operators: Top performing fabs involve operators more by providing timely, specific feedback on cycle time and other performance measures. In some fabs, this feedback is "real time"; that is, operators are able to identify lots that are falling behind schedule by looking at some sort of activity board or computer screen. Poor performers, although they seem to gather almost as much data as top performers, do not share as much of the information with the line operators.

We observed many simple, yet effective, ways that information can be communicated on the shop floor. For example, one fab put small LED counters on each stepper to count the number of operations during the shift. At a glance, operators in the area were able to measure their progress towards their productivity goals and, in some cases, identify equipment problems.

(2) Cycle time tracking and goal setting: Every fab that we visited keeps computerized records of each lot as it progresses through the fab. Data such as lot start time ("move-in time"), stop time ("move-out time"), machine used and operator performing the operation are logged at several points throughout the fabrication process. What differentiates fabs is what they do with this information. Top performing fabs treat cycle time as one of their primary performance metrics along with yield. They closely monitor cycle time in each processing area and investigate problems as they arise. They establish cycle time and productivity improvement goals and allocate the necessary resources to achieve these goals. In contrast, poor performers do not monitor cycle time as closely (in one case, not at all) and do not set improvement goals.

While tracking cycle time and setting improvement goals is no guarantee of success, it is interesting to note that 9 out of the top 10 fabs in CTPL performance treat cycle time as one of their primary metrics.

The level of detail, or granularity, of the tracking system can have a significant impact on its effectiveness. For example, several fabs we visited had combined the photolithography and etch steps into one "masking" step for tracking purposes. This made it difficult to determine actual load levels at individual work stations. It should be noted that this was a managerial decision and not an inherent limitation of the information technology employed.

Tracking cycle time can reveal problems not directly related to the process. For example, one fab manager told us how the fab's computer system became so overloaded that lot login at a particular workstation took 15 minutes while the actual processing time for that step took only about 5 minutes.

Modeling Cycle Time Performance [22]

In the foregoing we identified some of the factors that influence cycle time. But how much of an impact does, for example, process age have on cycle time? Does linking photo cells

22. This sub-section is modeled after "Semiconductor Yield Improvement: Results and Best Practice," S. Cunningham, C.J. Spanos, and K. Voros, Report CSM-10, Engineering Systems Research Center, University of California, Berkeley, CA 94720 (September, 1994)}

produce a measurable reduction in cycle time? In short, to what extent do the strategic and fab-level variables discussed influence cycle time performance? To better answer this question, we performed statistical analyses on the data collected. Our methodology and results are presented below.

Methodology

Using data from the mail-out questionnaire and the site visit interviews, we coded most of the strategic and fab-level variables identified above for each fab. Not all variables were included in our analysis. The inherent subjectivity of some variables made them undesirable, e.g., how does one assess the extent to which equipment modifications are made? Other variables were not readily available, e.g., not all fabs were able to provide an accurate estimate of the average number of "hot lots" in production. Our initial data set included 24 variables for 28 fabs. The variables are as follows:

Facility:

* Size - refers to the size of the cleanroom, measured in square feet. Cleanrooms smaller than 20,000 sq. ft. are defined as small; cleanrooms larger than 60,000 sq. ft. are defined as large.

* Class - refers to the cleanroom cleanliness level reported by the fab. A fab is class X if there are fewer than 10^X particles per cubic foot of cleanroom space. Two fabs employ standard mechanical interface (SMIF) boxes. These fabs are treated as class 0 fabs.

* Age - refers to the age of the facility. Fabs built before 1985 are labelled as 93Old94; fabs built between 1985 and 1990 are labelled as 93Mid94; those built after 1990 are labelled as 93New94.

Volume:

* Starts - refers to the average number of wafers started per week in the fab (considering all process flows).

* Flows - refers to the number of major process flows produced by the fab.

* Starts/Flow - refers to the average number of wafers started per week for each process flow in the fab.

* Products - refers to the number of active die types produced by the fab at the time our data was collected.

Process:

* Type - refers to whether the fab primarily produces bipolar or CMOS processes.

* Wafer Size - refers to the diameter, in inches, of wafers produced by the fab. All of our participants produce either four-, five-, or six-inch wafers.

* Age - refers to the time span, in months, between the first and last cycle time data point supplied for each fab's highest-volume process.

Product:

* Memory - refers to whether or not the fab produces memory devices.

* Logic - refers to whether or not the fab produces logic devices.

* Minimum feature size - refers to the minimum feature size, in microns, of the highest-volume product manufactured by the fab.

* Die Size - refers to the area of a the highest-volume die type, measured in square centimeters.

Market:

* ASIC - refers to whether or not the fab is primarily an ASIC (application specific integrated circuit) producer. "Yes" means that the fab builds to order; "No" means that the fab builds to plan.

* Captive - refers to whether or not the fab is "captive" in the sense that it primarily produces for a parent company. An affirmative response means that the fab is captive; a negative response means that the fab is a merchant producer.

Equipment:

* Availability - refers to the average availability of the bottleneck resource as reported by the fab. Availability is defined as the percentage of time that the machine is functioning properly -- either engaged in production or waiting to process a lot. We use this as an indicator of equipment reliability and maintenance practices.

* Use 5X Steppers - refers to whether or not the fab employs 5X steppers.

* Utilization - refers to the utilization of the 5X steppers. Utilization, for our purposes, is defined as the number of wafer operations per 5X stepper per day divided by 800. Values of "NA" indicate fabs that do not use 5X steppers.

* Automation - measures the extent to which the fab has automated functions. We considered four areas: automated material handling, linking of photolithography cells, automated recipe download, and automated data entry. For each area, a fab was given a score of one if this type of automation had been introduced and a score of zero otherwise. The automation variable listed is the sum of these scores. "None" indicates a total score of 0; "Low" indicates a total score of 1; "Med" indicates a total score of 2; "High" indicates a total score of 3; and "V. High" indicates a total score of 4.

Production Control:

* Shop-Floor - refers to whether or not the fab has an effective shop-floor control system.

* Planning - refers to whether or not the fab has an effective production planning system.

* CT goals - refers to whether or not the fab treats cycle time as one of its primary performance metrics and sets improvement goals for this metric.

* OTD goals - refers to whether or not the fab treats on-time delivery as one of its primary performance metrics and sets improvement goals for this metric. Table 3.5.3 placed at the end of this section displays the values of these variables for each fab.

For the purposes of this analysis, we define *CTPL* as the cycle time per mask layer averaged over the last year for which data is available and averaged over all process flows, weighted by volume. Similarly, we define *RCTPL* as the percentage quarterly improvement (i.e., reduction) in *CTPL*, averaged over the last year for which data is available. Our goal was to find a small set of independent variables that could explain the variation in *CTPL* performance and *RCTPL* performance of our participants.

The model underlying our analysis is that *CTPL* is a function of some strategic and fab-level decision variables. We assume a simple linear model of the following form:

$$CTPL = X\,B + e$$

where X is a matrix of variables including some subset of the 24 variables listed above, and e is an error term. We assume the same type of linear model for *RCTPL*, but we allow for the possibility that a different subset of the original 24 variables will explain variations in performance. We used linear regression to determine which factors, elements of the X matrix, have the most influence on *CTPL* and *RCTPL*.

Data and Caveats

Several caveats are in order before we present our results. First, our sample size is relatively small, so it is difficult to draw many general conclusions or predict performance based on the proposed model. Small sample size also increases the influence that individual observations have on the results, i.e., it makes our model more susceptible to distortions from "outliers."

Second, some of the variables that we measured are highly subjective. We made every effort to minimize the use of subjective variables and to ensure their accuracy when we did use them.

A third issue is that measurements were taken during different time periods. One could argue that this gives an unfair advantage to fabs that were studied more recently because they have had more time to improve. However, since we are analyzing practices within a certain time frame and their effect on performance in the same time frame, the results should still be valid. To help guard against this kind of bias, we defined a variable that measures the difference between each fab's observation window and the earliest observation window. With these caveats in mind, we can now discuss our findings.

Results: Mean Cycle Time

Originally, we included all of the variables in our design matrix, X. Statistical analyses revealed a clear bifurcation in the data: fabs that use 5X stepper technology and fabs that do not. Four out of the six fabs in our study that do not use 5X stepper technology exhibited higher-than-average cycle times; five out of six are bipolar producers; all six produce logic devices; and all six have little or no automation. Because of these significant differences, we chose to exclude these six fabs from our analysis.

Statistical analysis of the 22 remaining fabs revealed a small set of significant variables that describe a large proportion of the CTPL performance variation. The variables are: minimum feature size, automation, production planning, and die size (all defined above). The model can be expressed as

$$CTPL = 93.00 - 0.85\,(\text{Min feature size}) - 0.25\,(\textit{Automation}) - 0.50\,(\textit{Production Planning}) + 0.47\,(\textit{Die size}).$$

With this four-variable model, we are able to account for approximately 65 percent of the variation in the CTPL performance of the 22 fabs that use 5X stepper technology. More detailed results are reported in Table 3.5.1. The high F value and R-square value indicate that the model provides a good fit, and the T values for each of the coefficients indicate that each one is statistically significant.

There is a negative association between minimum feature size and CTPL, as indicated by the negative sign on the parameter estimate. This suggests that as the minimum feature size increases, CTPL decreases. In other words, cycle time is longer for products with smaller line widths. This seems reasonable in light of our earlier discussion: other things being equal, smaller minimum feature sizes require more time at the photolithography station which is typically the fab bottleneck.

The analysis indicates a negative association between automation and CTPL; that is, cycle time decreases as the level of automation increases. This result is consistent with our expectations. Similarly, the negative coefficient for production planning suggests that cycle time decreases as the effectiveness of the production planning system increases. This is certainly consistent with our discussion above.

Die size is positively associated with CTPL; that is, CTPL increases as chip size increases. This may be due to the fact that newer processes tend to be built on larger chips. As the process matures, the process will go through successive "shrinks," squeezing the circuitry into a smaller space.

In general, the results of our statistical analysis are encouraging. They suggest that, as expected, cycle time performance is associated with a number of decision variables concerning technology, market, equipment, etc. The decision of whether or not to use 5X steppers -- and other decisions that may be linked to this -- appear to be significant.

The mean CTPL model provides a good fit and suggests that some factors that are beyond an individual fab's control will play a significant role in cycle time performance (e.g., minimum feature size and die size). This model also demonstrates, however, that fab-level decisions play an important role. Effective production planning and judicious automation can significantly improve cycle time performance. What is perhaps surprising is the absence of some variables from the model such as number of process flows and 5X stepper utilization. It is interesting to note that the variable included to account for non-contemporaneous observation windows provided little explanatory power in our model. However, there is still a significant portion of the variation in cycle time performance that remains to be explained. This suggests that some other variables play an important role.

Results: Cycle Time Improvement Rate

Measuring the rate of cycle time improvement is a challenging task. Many participants experience a sharp drop in cycle time when improvement projects are undertaken, followed by steady, but much slower, decreases in cycle time. For example, one fab reported a rapid, substantial cycle time improvement as a result of installing linked photo cells. While they continue to make improvements in their cycle time performance, we would not expect the rate of improvement to remain high. Indeed, as more improvements are made, each incremental step becomes

Table 3.5.1: Results of Regression Analysis
Dependent Variable: CTPL (mean cycle time per layer)

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Value	Prob > F
Model	4	5.26383	1.31596	7.801**	0.0009
Error	17	2.86770	0.16869		
C Total	21	8.13153			

Root MSE	0.41072	R-square	0.6473
Dep Mean	2.89803	Adj R-sq	0.5644
C.V.	14.17229		

Parameter Estimates

Variable	DF	Parameter Estimate	Standard Error	t for $H0$: Parameter	Prob ≥ $\|t\|$
INTERCEPT	1	3.991687	0.39792486	10.031	0.0001
Minimum Feature Sz.	1	-0.849477	0.29959293	-2.835**	0.0114
Automation	1	-0.249664	0.09128999	-2.735**	0.0141
Production Planning	1	-0.497900	0.22071116	-2.256**	0.0375
Die Size	1	0.468993	0.22488001	2.086*	0.0524

Notes:
** significant at the 95% level
* significant at the 90% level

more difficult.

The same caveats made above regarding the data apply here as well. In addition, one fab (the worst CTPL performer) was not able to supply enough cycle time data to reasonably calculate the rate of improvement. Thus, for this analysis we are limited to only 21 fabs.

Statistical analysis revealed two (somewhat) significant variables in terms of explaining the variation in RCTPL performance. These variables are: number of products and CT goals. The model can be expressed as

$$RCTPL = 9.42E{-}03 + 3.28E{-}02\,(\,CT\ goals\,) - 9.15E{-}05\,(\,number\ of\ products\,).$$

With this two-variable model, we are able to describe approximately 21 percent of the variation in the RCTPL performance of the 21 fabs under consideration. More detailed results are reported in Table 3.5.2. The relatively small F value and low R-square value indicate that this model does not provide a particularly good fit. However, valuable insights can be still gained by studying the signs of the parameter estimates.

Cycle time tracking and goal setting appear to have a positive effect on cycle time improvement. This is certainly consistent with our observations. It is difficult to accurately assess the magnitude of the effect of this variable, but according to the model, monitoring cycle time and setting improvement goals will reduce cycle time by approximately 3.3 percent per year. Given that the average cycle time improvement of the fabs surveyed is less than 0.2 percent per year, this result is significant.

The negative sign on the parameter estimate for number of products suggests that as the number of products increases, the rate of cycle time reduction decreases. This seems reasonable given that, other factors being equal, more products will generally add complexity to the manufacturing process: more machine setups, greater variability in terms of product demand, etc. However, the small coefficient (9.15E-05) suggests that only a very large number of products will have a significant impact on cycle time.

Although these results are not very conclusive in a statistical sense, they are intuitively appealing. The analysis suggests that sustained, long-term cycle time improvement is not only a result of automation and technological innovation but also a result of organizational practices. Tracking cycle time and setting improvement goals appears to be one of the primary determinants of cycle time improvement. Other factors, such as number of products, may make improvement hurdles higher or lower, but they do not make a significant difference by themselves. The results also suggest that some other factors not included in our model play a role in cycle time improvement.

Conclusion

Short cycle time is important because it indicates an efficient fab and because it improves responsiveness to customer demand. In our last report, we concluded that cycle time is influenced by many factors beyond the control of individual fabs but that there are many fab-level practices that can significantly improve cycle time performance. Studying 14 more fabs and

Table 3.5.2: Results of Regression Analysis
Dependent Variable: RCTPL (cycle time improvement rate)

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Value	Prob > *F*
Model	2	0.00800	0.00400	2.431+	0.1163
Error	18	0.02962	0.00165		
C Total	20	0.03762			

Root MSE	0.04056	R-square	0.2127
Dep Mean	0.01902	Adj R-sq	0.1252
C.V.	213.21455		

Parameter Estimates

Variable	DF	Parameter Estimate	Standard Error	*t* for *H*0: Parameter	Prob > |*t*|
INTERCEPT	1	0.009420	0.01528995	0.616	0.5455
CT Goals	1	0.032822	0.01841973	1.782*	0.0916
Products	1	-0.000091502	0.00005933	-1.542+	0.1404

Notes:

* significant at the 90 percent level

+ significant at the 75 percent level

performing statistical analyses has reaffirmed these conclusions.

We have observed that fabs achieving good cycle time performance have learned to reduce variability in the manufacturing process and regulate the workload at the bottleneck workstation(s). They have done this by improving the starts schedule through effective production planning; controlling the flow of WIP, using Kanbans or other dispatching methods; and improving information flows by collecting "good" information and communicating it to those who can use it.

We have observed that sensible automation, such as robotic linking of photolithography cells, has a substantial, positive effect on cycle time performance.

Our statistical model of cycle time performance supports these observations and our intuition. First, we observed a clear split in the data between those who use 5X steppers and those who do not. This is perhaps indicative of some high-level, strategic decisions about technology, market, etc. Second, we found a four-variable model that describes a significant proportion of the cycle time performance variation among fabs that use 5X steppers. The model suggests that some "strategic" decisions (minimum feature size and die size) and fab-level practices (automation and production planning) have an impact on cycle time performance.

We also found evidence that cycle time improvement is driven by fab-level practices, specifically, monitoring cycle time and setting improvement goals. Although these results are encouraging, much remains to be explained. By studying more fabs and identifying additional decision variables and practices, we hope to narrow the gap between what our theory explains and what we observe in practice.

Table 3.5.3. Factors that Influence Cycle Time -- Fab Profiles

Fab ID	CTPL (mean)	RCTPL (improve (rate)	FACILITY Size	FACILITY Class	FACILITY Age	WSPW	VOLUME No. of Flows	VOLUME Starts Per Flow	No. of Die Types
B5	2.38	-0.01	Small	3	Old	1854	3	618	45
L4	3.27	0.02	Med	2	Mid	2798	4	700	50
B3	1.34	0.05	Med	2	Old	11027	6	1838	180
L8	2.73	0.02	Med	0	Mid	4538	1	4538	5
M3/L9	3.15	-0.01	Large	2	Mid	13883	55	252	320
L6	3.31	0.02	Large	3	Old	5128	12	427	200
M4	3.20	0.01	Large	2	Mid	1364	5	2273	12
B1	3.04	-0.06	Large	1	Old	2726	3	909	65
M5/L5	2.45	-0.01	Med	0	New	7312	3	2437	40
L11	2.49	-0.04	Small	0	Old	1879	7	268	600
L3	3.20	0.14	Med	1	Mid	590	2	295	13
L10	2.73	-0.03	Small	2	Old	301	2	151	10
L1	2.90	0.00	Med	1	Mid	3019	5	604	85
M6	2.01	0.01	Large	1	New	7191	3	2397	15
M7/L12	2.29	0.10	Small	0	Mid	1814	9	202	85
L7/B2	2.71	0.00	Small	2	Mid	2512	10	251	400
L13	3.35	0.02	Med	1	Mid	3929	5	786	150
B4	3.85	-0.07	Small	1	Mid	821	4	205	61
M8/L14	3.69	0.07	Med	1	Mid	6243	3	2081	140
M9	2.97	-0.01	Med	1	New	1214	2	607	3
B6	2.26	0.05	Med	2	Old	2676	10	268	212
M2/L2	2.89	-0.02	Med	2	Mid	10237	4	2559	80
L15	3.41	-0.02	Med	0	Mid	3100	3	1033	15
M1	3.40	0.04	Med	1	Mid	5162	1	5162	6
B7	3.91	-0.06	Med	1	Mid	1900	5	380	200
B8	3.18	0.02	Med	2	Old	11088	5	2218	130
L16	2.10	0.05	Med	1	Old	6601	3	2200	50
M10	4.15	NA	Med	0	Mid	12507	7	1787	10

Table 3.5.3. Factors that Influence Cycle Time -- Fab Profiles (cont.)

Fab ID	PROCESS Type	Wafer Size	Age	PRODUCT Memory	Logic	Minimum Feat.Sz.	Die Size	MARKET ASIC	Captive
B5	Bip, CMOS	4	27	No	Yes	3.00	0.15	No	No
L4	CMOS	6	50	No	Yes	0.90	0.48	No	No
B3	Bipolar	4	45	No	Yes	2.00	0.03	No	No
L8	CMOS	6	64	No	Yes	0.90	1.31	No	No
M3/L9	CMOS	6	27	Yes	Yes	0.70	0.83	No	No
L6	CMOS	5	54	No	Yes	1.20	0.88	No	Yes
M4	CMOS	6	23	Yes	No	0.70	0.82	No	No
B1	Bip, CMOS	5	45	No	Yes	0.00	0.21	No	Yes
M5/L5	CMOS	6	24	Yes	Yes	0.80	0.45	No	No
L11	CMOS	6	78	No	Yes	1.50	0.98	Yes	No
L3	CMOS	6	14	No	Yes	0.70	1.91	No	Yes
L10	CMOS	5	23	No	Yes	1.50	1.43	No	Yes
L1	CMOS	6	21	No	Yes	1.00	0.74	Yes	No
M6	CMOS	6	12	Yes	No	0.55	0.57	No	No
M7/L12	CMOS	6	30	Yes	Yes	0.80	0.42	No	No
L7/B2	CMOS	5	12	No	Yes	1.20	0.36	No	No
L13	CMOS	5	30	No	Yes	0.90	0.70	Yes	No
B4	BiCMOS	5	36	Yes	Yes	1.50	0.52	No	No
M8/L14	CMOS	6	27	Yes	Yes	0.80	0.23	No	No
M9	CMOS	6	27	Yes	No	0.80	0.83	No	Yes
B6	Bipolar	5	48	Yes	Yes	2.50	0.18	No	No
M2/L2	CMOS	6	27	Yes	Yes	0.80	0.82	No	Yes
L15	CMOS	6	5	No	Yes	0.60	0.43	No	No
M1	CMOS	6	12	Yes	No	0.80	0.53	No	No
B7	BiCMOS	6	54	No	Yes	2.00	0.03	No	No
B8	Bipolar	4	34	Yes	Yes	5.00	0.04	No	No
L16	CMOS	5	32	No	Yes	1.20	0.31	No	No
M10	CMOS	6	37	Yes	No	0.70	0.49	No	Yes

Table 3.5.3. Factors that Influence Cycle Time -- Fab Profiles (cont.)

Fab ID	EQUIPMENT			PRODUCTION CONTROL			
	Avail.	Use 5X Steppers	Stepper Util.	Automation	Shop-Floor	Planning	CT Goals	OTD Goals
B5	94.0	No	NA	None	Yes	No	Yes	Yes
L4	92.0	Yes	0.32	Low	Yes	No	No	No
B3	90.0	Yes	0.84	Med	Yes	Yes	Yes	Yes
L8	90.0	Yes	0.59	High	No	No	No	No
M3/L9	70.0	Yes	0.40	Med	No	No	Yes	No
L6	88.0	Yes	0.41	Med	Yes	No	Yes	Yes
M4	90.0	Yes	0.66	V.High	No	No	No	No
B1	80.0	No	NA	Low	No	Yes	No	No
M5/L5	85.0	Yes	0.70	High	Yes	No	Yes	Yes
L11	76.0	Yes	0.18	Med	Yes	Yes	Yes	Yes
L3	91.0	Yes	0.28	Med	Yes	Yes	Yes	No
L10	80.0	Yes	0.02	Low	Yes	Yes	Yes	No
L1	80.4	Yes	0.47	Low	Yes	Yes	Yes	Yes
M6	91.0	Yes	0.92	V.High	Yes	Yes	Yes	No
M7/L12	83.0	Yes	0.33	Med	No	Yes	Yes	Yes
L7/B2	85.0	Yes	0.26	None	No	No	No	No
L13	92.5	Yes	0.30	Low	Yes	No	No	Yes
B4	70.0	No	NA	Low	Yes	Yes	Yes	Yes
M8/L14	93.0	Yes	0.58	Low	Yes	No	Yes	No
M9	92.8	Yes	0.52	Low	Yes	No	No	Yes
B6	98.0	No	NA	None	No	No	Yes	Yes
M2/L2	85.0	Yes	0.63	High	Yes	No	No	No
L15	69.6	Yes	0.42	Low	Yes	No	No	Yes
M1	82.2	Yes	0.36	Med	No	No	Yes	Yes
B7	60.9	No	NA	None	Yes	Yes	Yes	No
B8	98.5	No	NA	None	No	Yes	Yes	No
L16	97.2	Yes	0.40	Low	No	No	Yes	No
M10	94.0	Yes	0.76	Low	No	No	No	Yes

3.6. Computer-Integrated Manufacturing and Automation
by Chien Hwa Wang and Robert C. Leachman

As emphasized in previous sections, data collection and analysis are key to performance in the areas of process control, yield improvement and equipment efficiency. The quality and scope of a fab's information systems are thus critical to its performance. In our fab visits, we have observed a trend toward increased material handling automation, promising increased labor and equipment productivity and increased yields by making manufacturing more mistake-proof and repeatable. In this section we correlate the performance data with information system and automation practices in order to identify those practices that differentiate performance among our participants.

Tables 3.6.1 - 3.6.3 placed at the end of this section present summaries of computer-integrated manufacturing (CIM) and automation practices of our participants. Separate tables are presented for memory, CMOS logic and MSI fabs. In each table, general categories of CIM and automation practices include Computerized Applications, Information Handling Automation, and Material Handling Automation. There are several subcategories under each general category, each subcategory listing several practices. For each fab, in each practice area, we have given a high, medium or low rating of fab practices during the time frame of performance data. The rating indicates the intensity or sophistication of the practice, according to our understanding acquired during the site visit. In some cases, we have shown a transition score such as "L->H" indicating the fab implemented or substantially upgraded this practice in the middle of the time frame. It must be acknowledged that, by the time of our site visit or subsequent to it, many of our participants upgraded their practices from what is shown in the table. It is also possible that some practices for some fabs were omitted or mis-rated in our analysis because we missed them in the discussions during our visit. In any event, the tables show our best judgement of fab practices during the time frame of the performance data.

In the Computerized Applications category are subcategories for Lot Operations, Equipment and Process Tracking, Scheduling, Yield Analysis, and Others. In the Information Handling Automation category are subcategories for Data Capture, Data Download and Monitoring. In the Material Handling Automation category are subcategories for Step Automation, Intrabay Automation and Interbay Automation. We briefly explain each practice as follows.

In the Lot Operations subcategory, *WIP tracking* refers to the activity of recording the initiation and completion of processing operations on production lots. All of our participants receive at least a medium score in this practice; some receive a "high" score if the information is more complete, e.g., which machine and which operator performed the processing, many detailed operations are recorded instead of a smaller number of aggregate ones, both move-in and move-out times are recorded, etc. The *recipe management* practice indicates the extent to which the machine recipe to use is displayed on-line to the operators once a lot is selected for processing. The *reticle tracking and verification* practice means the operator is informed on-line of the storage location and reticle number to use at a lithography step, and, once the reticle is selected, the correctness of the selection is verified by reading a bar code on the reticle. *Bay or block controllers* assign machines to lots selected for processing and display status of all lots and machines in a process block.

In the Equipment and Process Tracking subcategory, *equipment tracking* refers to the computerized storage of machine status (production, idle, down), with reason codes or subclassifications for down and idle states. *EDC (engineering data collection)* refers to the computerized storage of process and equipment measurements. *SPC* refers to computerized statistical process control. The *trouble-shooting* practice refers to on-line display of out-of-control action procedures in support of SPC. *In-line wafer maps* indicates that visual displays of the results of wafer inspections for defects are available on-line.

In the Scheduling subcategory, the *on-line lot scheduling* practice refers to computerized display of recommended sequence to process waiting production lots. The *Kanban* practice refers to a computerization of just-in-time control rules that inhibit processing of lots for which downstream WIP exceeds specified limits while encouraging the processing of lots with low downstream WIP. The subsequent rows in this subcategory indicate the extent of computerization of preventive maintenance scheduling, shift scheduling, production planning and capacity planning, while the last practice in this subcategory indicates the reported extent of use of computerized simulation of fab operations.

In the Yield Analysis subcategory, the *end-of-line wafer maps and bit maps* practice indicates whether or not such maps are available on-line. The *integrated production, EDC and yield database* practice indicates the extent to which such data is readily and timely available in a single database suitable for the application of statistical analysis. The *statistical analysis of yield vs. in-line data* practice indicates the extent to which computerized analysis of this type is carried out, while the *statistical tools* practice indicates the extent to which such tools are directly connected to the database, as opposed to requiring the engineer or analyst to download data from the database to some other environment where statistical analysis tools are available. The *statistical analysis reports* practice indicates the extent to which regular, formal reports of the results of correlations of yield vs. in-line data are published, while the *ad-hoc query* practice indicates the relative ease with which engineers or analysts can make new queries against the database for statistical analysis.

In the Others subcategory, practices are listed for computerized tracking and purchasing of raw materials, computerized document control systems, and computerized costing and financial valuations.

In the Data Capture subcategory, there are practices for the extent of automating the upload to databases of metrology data and process (EDC) data, as opposed to requiring operators to key such information into a central tracking system. There is a practice for automated SPC data entry, indicating the extent to which data entry for SPC is automatically performed from EDC. There are also practice areas for automating the upload of in-line electrical test and sample probe results. The *automated equipment tracking* practice indicates the extent to which machine logs or sensor readings (in a summarized and readable form) are automatically collected in a central database. The *automated equipment tracking data entry* practice indicates the extent to which the operator is assisted in performing such tracking, e.g., automatically prompting the operator to fill in the tracking screen when a state change is detected, automatically filling in the machine ID, etc. The automated metrology equipment status upload is a similar practice for metrology equipment.

In the Data Download subcategory, the *auto-recipe download* practice indicates the extent to which process recipes are automatically input to processing machines once a lot or batch has been selected for processing. The *auto sanity-check* practice indicates the extent to which there are are computerized checks of the machine and lot selected to insure against misprocessing.

In the Monitoring subcategory, the *process out-of-control alarms* practice indicates the extent to which SPC OOC events trigger alarms or messages to responsible individuals as well as disabling the movement of lot and/or use of the equipment until control is restored. The *machine trouble or idle alarms* practice indicates the extent to which machines are equipped with sensors and with audio or visual signals that alert staff to the need for maintenance or service or the impending completion of an operating cycle.

In the Step Automation subcategory, the *SMIF* practice indicates the extent to which microenvironments for machines and lots equipped with standard mechanical interface (SMIF) technology have been applied. The remaining practices in this category refer to the application of robotics or other means to automate wafer handling in and out of processing machines. There is one overall practice for the extent of load/unload automation, and then more specific practices concerning the application of robots to wet benches, plasma etch, diffusion furnaces, and other deposition areas. There also is the *linked lithography* practice, indicating the extent to which coat, expose and develop operations have been linked up into a single operation using tracks and elevators or robotic arms.

Our sample of participants does not include any fabs with full intrabay automation, although we have observed other more recent fab lines equipped with such automation. We do have a few participants that have taken steps toward intrabay automation, as shown in the Intrabay Automation subcategory. Specifically, we have a practice for automated location of lots and reticles, in which racks for storage of same are electronically linked, and the physical locations of the lot and reticle to select are indicated to the operator by the computer. We also have a practice for automated retrieval and storage of reticles using a stocker in the photo bay.

In the Interbay Automation subcategory, the automation system may be implemented either using an overhead lot railroad connecting stockers serving each equipment bay, or using automated guided vehicles (AGVs) traveling between the stockers. We have observed both kinds in operation among our participants, and so we have practices for each.

At the bottom of the tables, the rankings of fab performance in the various technical metrics are shown. Numerical scores presented in Chapter 2 have been converted into high, medium or low scores according to rankings made by type of fab. For convenience, fab characteristics (wafer starts, utilization, number of process flows, number of die types, bottleneck equipment type) discussed in Chapter 2 also are included at the bottom.

In order to perform a correlation analysis of CIM and automation practices with technical performance, we converted the high/medium/low rankings into 3/2/1 numerical scores, respectively. For fabs that made a transition from one ranking to another, we used an average score, e.g., a M->H ranking was given a score of 2.5. Tables 3.6.4 - 3.6.5 present the results of this analysis.

To appreciate the relative impact of different practice areas, we have correlated aggregate scores in each subcategory with the fab technical performances, as displayed in Table 3.6.4. The

aggregate score for each fab in each subcategory is simply the sum of the fab's scores for each practice in the subcategory. Table 3.6.5 displays the results of correlation analysis of individual CIM and automation practices vs. fab performance in the technical metrics. Positive correlations greater than 0.35 are displayed in bold face in the tables.

The most arresting result in Table 3.6.4 is that the automation of information handling provides substantial positive impacts on line yield, machine throughput, labor productivity, cycle time and integrated throughput. Step-level material handling automation also significantly benefits these categories. These forms of automation make manufacturing far more mistake-proof, they make data collection far more accurate and timely, and they relieve operators of considerable workload, thereby enabling them to keep machines more continuously engaged in processing.

Correlations of performance with steps taken toward intrabay material handling automation are much weaker. Some positive correlations show up for interbay automation, but we conjecture that this is an artifact of our data set, in which fabs with interbay automation are typically also fabs with strong practices in the automation of information handling and in yield analysis.

Correlations between the practice areas in our data set are displayed in Table 3.6.6. As can be seen, interbay automation is strongly correlated with all of the information automation subcategories. There are other important correlations as well. Information linkages to processing machines enable a number of different improvements that end up highly correlated in our data set. For example, SECSII interfaces to processing equipment enable auto-recipe download, auto-capture of process data, auto process monitoring, as well as automation of the material handling aspects of a process step. Thus these four subcategories are highly correlated in our data as well.

Turning to the other subcategories in Table 3.6.4, those fabs with computerized yield analysis tend have the lowest defect densities. More sophisticated applications for lot operations, particularly recipe management and reticle management, tend to improve equipment throughput and reduce cycle time.

No significant positive correlations show up for Scheduling, for Equipment and Process Tracking, or for the Other subcategory of computerized applications. For the Scheduling subcategory, fabs strongest in this regard in our sample tend to be ASIC fabs which have great technical disadvantages (small lot sizes, many process flows and die types, etc.) for the achievement of high technical performance. Sophisticated, computerized scheduling serves to help such fabs achieve superior levels of on-time delivery. The benefits of good production planning also show up most strongly in on-time delivery performance and in lower downstream inventories, rather than in the technical categories correlated here.

For the Equipment and Process Tracking and the Other subcategories, the fact that almost all fabs in our survey include such applications in their information systems means that our tabulation of their mere existence cannot distinguish performance. What is more significant is the *quality* of such applications. As indicated in Table 3.6.5, providing more automated equipment tracking data entry is strongly associated with improved line yields, equipment throughput and labor productivity. Automated capture of engineering data also is strongly correlated with improved line yield, stepper throughput and labor productivity.

Examining the results for correlations of individual practices in Table 3.6.5, under Yield Analysis we find that defect density performance is most profoundly influenced by the maintenance of an integrated production, EDC and yield database. Intense and routine performance of statistical analysis on this database between yield and in-line data also is strongly correlated with defect density reduction. Along with the availability of end-of-line wafer maps and bit maps, these same two factors show up strongly with respect to integrated 5X stepper throughput, our measure of overall fab productivity.

In the Data Capture subcategory, auto-upload of metrology and process data and auto-entry of SPC data are correlated with integrated stepper throughput, as are automated equipment tracking or auto-entry of equipment tracking data. These forms of information automation also are strongly correlated with increased labor productivity.

Auto-recipe download shows perhaps the highest positive correlations of all practices. Line yields, equipment throughputs and labor productivities are all substantially enhanced by this practice. A more modest practice that provides most of the mistake-proofing benefits of auto-recipe download is the automated sanity-check of machine and lot; this practice also shows strong correlations with line yields, equipment and labor productivities.

In the Monitoring subcategory, both Automated process and equipment alarms are strongly correlated with defect density performance. Machine trouble and idle alarms are associated with good line yield and with equipment and labor productivity.

In the Step automation subcategory, the application of robotics tends to improve line yields and equipment and labor productivity. Linked lithography cells also has a positive impact on die yield.

As discussed above, interbay automation is strongly correlated with technical performance in our data, but we believe this reflects correlations in our data set between interbay automation and other practices that more directly influence the metrics.

A final correlation analysis we ran compared technical performance to whether or not the information systems were primarily commercial systems or primarily home-grown. No significant correlations were found, i.e., we have examples in our database of excellent CIM and automation practices based on home-grown systems as well as on commercial systems.

In summary, the most important benefits of CIM in semiconductor manufacturing concern the automation of information handling. This serves to (1) make manufacturing mistake-proof, (2) collect more accurate data in a more timely fashion, enabling more productive use of engineering resources to respond to problems and to improve manufacturing, and (3) relieve manufacturing of much time-consuming effort dealing with data retrieval and data entry. Material handling automation would seem to have the highest payoff at the step level rather than at the bay or interbay level. Again the focus on step automation serves to make manufacturing mistake-proof, and it serves to make the process more repeatable and amenable to analysis.

Another key benefit of CIM concerns defect density reduction. The maintenance of an integrated production, engineering and yield database, against which statistical analysis of yield data vs. in-line data is routinely performed, is a powerful technique for defect density reduction.

Table 3.6.1 CIM and Automation Practices in the Memory Fabs

Fab ID	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
COMPUTERIZED APPLICATIONS										
Lot Operations										
WIP tracking	M	H	H	H	H	H	M	M	M	H
Recipe management	H	H	H	H	H	H	H	L->M	L	L
Reticle tracking and verification	L	L	H	L	H	L	L	L	L	L
Bay or block controller	L	M	L	M	L	L	L	M	L	L
Equipment & Process Tracking										
Equipment tracking	H	H	L	H	H	H	H	H	H	H
Engineering Data Collection	H	H	H	H	M	H	M	H	H	H
Statistical Process Control	H	H	L	H	H	H	H	H	H	H
Trouble-shooting assistance	L	L	L	L	L	L	L	L	L	L
In-line wafer maps	H	L	L	L	L	L	L	L	L	H
Scheduling										
On-line lot scheduling	H	L	L	L	H	L	H	H	L	L
Kanban	L	L	L	L	L	L	L	L	L	L
Preventive maintenance scheduling	L	L	L	L	L	L	L	L	L	L
Shift scheduling - fab wide	L	L	L	H	H	L	L	H	L	L
Shift scheduling - fab start only	L	L	L	L	L	H	H	L	L	L
Production planning	H	L	L	H	H	L	L	H	L	L
Capacity planning	L	L	L	H	H	L	H	L	L	L
Fab simulation	L	L	L	L	L	L	L	L	L	L
Yield Analysis										
End of line wafer maps & bit maps	H	H	H	H	M	H	L	L	H	H
Integrated prod'n, EDC, & yield DB	H	H	H	H	H	H	H	L	L	H
Relational database for analysis	H	L	L	L	H	L	H	L	L	L
Stat analysis of yield vs. in-line data	H	H	H	H	M	H	H	L	L	H
Stat tools connected to analysis DB	H	H	L	L	H	H	L	L	L	L
Statistical analysis reports	H	H	L	H	M	H	H	L	L	L
Ad-hoc query capability for analysis	H	L	L	L	H	L	H	L	L	L
Others										
Materials purchasing & order tracking	H	H	L	L	L	H	L	H	H	H
Computerized doc control systems	L	H	L	L	L	L	L	L	H	L
Costing & financial valuations	H	L	L	L	L	H	L	L	L	L
INFORMATION AUTOMATION										
Data Capture										
Auto-upload metrology data	L	M	L	H	L	M	L	H	L	H
Auto-upload process EDC	L	M	L	H	H	H	L->M	M	L	H
Auto SPC data entry	L	H	L	L	H	L->M	L	M	L	L

Table 3.6.1 CIM and Automation Practices in the Memory Fabs (cont.)

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
Data Capture (cont.)										
Auto-upload in-line elec test results	M	L	L	H	L	L	L	L	L	L
Auto-upload sample probe results	L	L	L	H	L	L	L	L	L	L
Auto WIP tracking data entry	L	H	L	H	H	H	L	H	L	H
Auto equipment tracking	L	M	L	M->H	M	L	L	L	L	M
Auto equip. tracking data entry	L	H	H	H	H	H	L	L	L	H
Auto metrology equip. status upload	L	H	L	L	L	L	L	L	L	H
Data Download										
Auto-recipe download	L	H	L	H	H	H	M	M	L	L
Auto sanity-check machine <-> lot	L	H	H	H	H	H	L	H	L	H
Monitoring										
Process out of control alarms	H	L	L	L	L	H	L	L	L	H
Machine trouble or idle alarms	M	H	H	H	L	H	L	L	L	M
MATERIAL HANDLING AUTOMATION										
Step Automation										
SMIF	L	L	L	L	H	L	L	L	L	L
All machines robot load/unload	L	M	L->M	M	H	M->H	L	L	L->M	L
Wet bench robot	L	L	H	H	L	L	L	L	L	L
Linked or robotic lithography	L	H	L	H	H	H	L	L	L	L
Diffusion furnace robot	L	H	L	L	L	H	H	L	H	L
Other deposition area robot	L	L	L	L	L	H	L	L	L	L
Etch area robot	L	L	L	L	L	H	L	L	L	L
Intrabay Automation										
Auto-locate lot and reticle	L	L	L	L	H	L	L	L	L	L
Auto reticle retrieval and storage	L	L	L	L	L	L	L	L	L	L
Interbay Automation										
RR and stockers	H	H	L	H	L	H	L	M	L	H
AGVs and stockers	L	L	H	L	L	L	L	L	L	L
Performance										
Defect density	3	2.5	2.5	2.5	1	3	2	2	2	2.5
Line yield	2	3	3	3	2	3	1	1	1.5	2.5
Stepper throughput	1	2.5	2	2.5	2.5	3	1	2.5	1.5	2
Implanter throughput	2	2.5	3	2.5	2	3	2	2.5	1	1.5
Metal throughput	1	2	2.5	2	3	2	2	3	NA	2
DL productivity	1.5	2	2	3	1.5	3	1.5	1.5	1	3
TL productivity	1.5	2	1.5	3	1.5	2.5	1	1.5	1	2.5
Cycle time	2	1.5	2	2	2.5	3	2.5	2	2	1
Integrated yield	3	2.5	3	3	1	3	1	1	1.5	3
Integrated stepper throughput	1.5	2.5	2.5	2.5	1.5	3	1	1	1.5	2.5

Note: NA - not available

Table 3.6.2 CIM and Automation Practices in the Logic Fabs

Fab ID	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
COMPUTERIZED APPLICATIONS																
Lot Operations																
WIP tracking	M	H	M	M	H	H	M	M	H	M	M	M	H	M	H	M
Recipe management	L	H	H	H	H	H	H	H	H	L	H	H	H	L->M	M	L
Reticle tracking and verification	L	L	L	L	H	L	L	H	H	L	L	L	L	L	L	L
Bay or block controller	L	M	L	L	L	L	L	L	L	L	L	L	M	M	L	L
Equipment & Process Tracking																
Equipment tracking	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
Engineering Data Collection	H	H	H	H	M	H	H	H	H	H	M	M	H	H	H	H
Statistical Process Control	H	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H
Trouble-shooting assistance	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
In-line wafer maps	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
Scheduling																
On-line lot scheduling	L	L	H	H	H	H	H	H	L	L	H	H	H	H	H	L
Kanban	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
Preventive maintenance scheduling	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Shift scheduling - fab wide	L	L	H	L	H	H	H	L	L	L	L	L	L	L	L	L
Shift scheduling - fab start only	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	L
Production planning	H	L	H	M	H	H	H	H	L	L	L	L	L	L	H	L
Capacity planning	L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H
Fab simulation	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
Yield Analysis																
End of line wafer maps & bit maps	L	H	H	H	M	H	L	H	H	H	M	L	L	L	L	L
Integrated prod'n, EDC, & yield DB	H	H	H	L	H	H	L	H	H	H	H	H	L	L	L	L
Relational database for analysis	L	L	H	0->H	H	H	L	H	L	H	H	H	H	L	H	H
Stat analysis of yield vs. in-line data	H	H	H	H	M	H	L	H	H	H	H	L	H	L	M	L
Stat tools connected to analysis DB	L	H	H	M	H	H	H	H	L	H	H	H	H	L	H	H
Statistical analysis reports	L	H	H	M	M	H	L	H	L	H	H	H	H	L	L	L
Ad-hoc query capability for analysis	L	L	H	M	H	H	H	H	L	L	L	H	H	H	L	H
Others																
Materials purchasing & order tracking	H	H	L	L	L	H	H	M	L	L	L	L	H	H	H	L
Computerized doc control systems	L	H	L	L	L	H	L	L	L	L	L	L	L	L	L	H
Costing & financial valuations	L	L	L	L	L	H	H	L	L	H	H	L	H	L	L	L
INFORMATION AUTOMATION																
Data Capture																
Auto-upload metrology data	H	M	M	L	L	M	L	L->M	L	L	L	L	M	H	L	L
Auto-upload process EDC	L	M	M	L	H	L->M	L	L	L	L	L	L->M	M	M	M	L->M
Auto SPC data entry	L	H	M	L	H	M	L	L	L	L	L	L	M	M	L	L->M

Table 3.6.2 CIM and Automation Practices in the Logic Fabs (cont.)

Data Capture (cont.)	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
Auto-upload in-line elec test results	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
Auto-upload sample probe results	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Auto WIP tracking data entry	L	H	M	L	H	L	L	L->M	L	L	H	L	M	H	L	M
Auto equipment tracking	L	M	M	L	M	L	L	L->M	L	L	M	L	L	L	L	M
Auto equip. tracking data entry	L	H	M	L	H	L	L	L	H	L	M	L	M	L	L	M
Auto metrology equip. status upload	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	M
Data Download																
Auto-recipe download	L	H	M	M	H	L->M	L	L->M	L	L	L	M	M	M	M	M
Auto sanity-check machine <-> lot	L	H	L	L	H	L	L	L	H	L	L	L	L	H	L	L
Monitoring																
Process out of control alarms	L	L	L	L	L	L	L	L								
Machine trouble or idle alarms	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
MATERIAL HANDLING AUTOMATION	H	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L
Step Automation																
SMIF	L	L	L	M	H	L	L	L	L	L	H	L	L	L	L	L
All machines robot load/unload	M	M	L	L	H	L->M	L->M	L->M	L->M	L	M	L->M	L	L	L	L
Wet bench robot	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	M
Linked or robotic lithography	H	H	L	L	H	H	L	H	L	L	H	L	L	L	L	L
Diffusion furnace robot	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L
Other deposition area robot	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Etch area robot	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Intrabay Automation																
Auto-locate lot and reticle	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
Auto reticle retrieval and storage	L	L	M	L	L	L	L	H	L	L	L	L	L	L	L	L
Interbay Automation																
RR and stockers	H->0	H	L	L	L	L	L	L	L	L	L	L	L	M	L	L
AGVs and stockers	L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L
Performance																
Defect density	2.5	3	2	2.5	2	2.5	1	3	3	1.5	2.5	1	1	2	1	2.5
Line yield	3	3	2	2.5	2.5	1.5	2	1	3	1.5	1	2	2	1.5	2	3
Stepper throughput	2	3	1.5	2	3	2	2	2.5	2.5	1	1	2	1.5	3	2	2
Implanter throughput	2.5	2.5	1	2	2	1.5	1	3	3	NA	NA	1	1	3	1	1.5
Metal throughput	2.5	2	1	2.5	3	3	1.5	3	2.5	1	2	2	1	3	1.5	2
DL productivity	2	3	1	1.5	2.5	1.5	2	2.5	3	1	1	2	1.5	2.5	1.5	2.5
TL productivity	2	3	1	2	2.5	1.5	2	2.5	3	1	1	2	1.5	2	1.5	2.5
Cycle time	2	2	2.5	1	2.5	2	2	2.5	2	2	2.5	3	1.5	1	1	3
Integrated yield	1	3	1.5	2	2.5	2	1.5	3	2.5	1	2	2	2	2	1.5	2.5
Integrated stepper throughput	3	3	2	2	3	2.5	1	2.5	3	1.5	2	1	2	2	1.5	3

Note: NA - not available

Table 3.6.3 CIM and Automation Practices in the MSI Fabs

Fab ID	B1	B2	B3	B4	B5	B6	B7	B8
COMPUTERIZED APPLICATIONS								
Lot Operations								
WIP tracking	M	M	H	M	M	M	M	M
Recipe management	L	H	H	L	L	L	L	L
Reticle tracking and verification	L	L	L	L	L	L	L	L
Bay or block controller	L	L	M	L	L	L	L	L
Equipment & Process Tracking								
Equipment tracking	H	H	H	H	H	H	H	H
Engineering Data Collection	L	H	H	M	L	H	M	M
Statistical Process Control	H	H	H	H	L	H	H	H
Trouble-shooting assistance	L	L	H	L	L	L	L	L
In-line wafer maps	L	L	L	L	L	L	L	L
Scheduling								
On-line lot scheduling	L	H	H	H	H	L	H	H
Kanban	L	L	H	L	L	L	L	L
Preventive maintenance scheduling	H	L	L	L	H	L	L	L
Shift scheduling - fab wide	H	H	L	H	L	L	L	L
Shift scheduling - fab start only	L	L	L	L	L	L	L	L
Production planning	H	H	H	H	H	L	H	H
Capacity planning	L	L	L	L	L	L	L	L
Fab simulation	L	L	L	L	L	L	L	L
Yield Analysis								
End of line wafer maps & bit maps	L	L	H	L	L	H	L	L
Integrated prod'n, EDC, & yield DB	L	L	L	L	L	L	L	L
Relational database for analysis	L	L	L	H	L	L	L	L
Stat analysis of yield vs. in-line data	L	L	L	L	L	L	M	M
Stat tools connected to analysis DB	H	H	L	L	L	L	L	L
Statistical analysis reports	H	L	L	H	H	L	L	L
Ad-hoc query capability for analysis	L	H	H	H	L	L	L	L
Others								
Materials purchasing & order tracking	L	H	H	H	L	H	H	H
Computerized doc control systems	L	L	L	L	H	H	L	L
Costing & financial valuations	H	H	H	H	H	L	L	L
INFORMATION AUTOMATION								
Data Capture								
Auto-upload metrology data	L	L	L	L	L	L	L	L
Auto-upload process EDC	L->M	L	M	L	L->M	L	L	L
Auto SPC data entry	L	L	L->M	L->M	L	L	L	L

Table 3.6.3 CIM and Automation Practices in the MSI Fabs (cont.)

	B1	B2	B3	B4	B5	B6	B7	B8
Data Capture (cont.)								
Auto-upload in-line elec test results	L	L	L	L	L	L	L	L
Auto-upload sample probe results	L	L	L	H	H	L	L	L
Auto WIP tracking data entry	L	L	H	M	L	L	H	H
Auto equipment tracking	L	L	M	M	L	L	L	L
Auto equip. tracking data entry	L	L	M	M	L	L	L	L
Auto metrology equip. status upload	L	L	L	L	L	L	L	L
Data Download								
Auto-recipe download	L	L	M	L	L	L	L	L
Auto sanity-check machine <-> lot	L	L	L	L	L	L	L	L
Monitoring								
Process out of control alarms	L	L	L	L	L	L	L	L
Machine trouble or idle alarms	L	L	L	L	L	L	L	L
MATERIAL HANDLING AUTOMATION								
Step Automation								
SMIF	L	L	L	L	L	L	L	L
All machines robot load/unload	L	L->M	M->H	L	L	L->M	L	L
Wet bench robot	L	L	H	L	L	L	L	L
Linked or robotic lithography	L	L	H	L	L	L	L	L
Diffusion furnace robot	L	L	H	L	L	H	L	L
Other deposition area robot	H	L	H	L	L	L	L	L
Etch area robot	L	L	L	L	L	L	L	L
Intrabay Automation								
Auto-locate lot and reticle	L	L	L	L	L	L	L	L
Auto reticle retrieval and storage	L	L	L	L	L	L	L	L
Interbay Automation								
RR and stockers	L	L	L	L	L	L	L	L
AGVs and stockers	L	L	L	L	L	L	L	L
Performance								
Defect density	2.5	1.5	1	1	2.5	3	1	1
Line yield	1	2.5	2	NA	1.5	3	1	1
Stepper throughput	NA	2	3	NA	NA	NA	NA	NA
Implanter throughput	1	2	2.5	1	1.5	1	1	1
Metal throughput	1	2	2.5	1	1	1	1	1
DL productivity	3	2	3	2	2	2	2	2
TL productivity	3	1.5	3	2.5	2	2	1	2
Cycle time	1.5	1.5	3	1	2	2	1	1
Integrated yield	NA	NA	NA	NA	NA	NA	NA	NA
Integrated stepper throughput	2	2	1	1.5	2.5	3	1	1

Note: NA - not available

Table 3.6.4 Correlations of CIM and Automation Practice Areas with Fab Performance

	Defect density	Line yield	Stpr tput	Imp tput	Met tput	DL prod	TL prod	Cycle time	Integ yield	Integ stpr tput
Computer Application - Lot Operations	0.194	**0.414**	**0.532**	**0.567**	**0.536**	0.269	0.253	**0.351**	**0.591**	0.306
Computer Application - Eqpt Tracking	0.023	0.212	-0.003	0.043	0.136	0.101	0.144	0.147	0.035	-0.060
Computer Application - Scheduling	-0.336	-0.304	0.057	-0.357	-0.090	-0.133	0.030	0.079	-0.283	-0.197
Computer Application - Yield Analysis	**0.411**	0.195	-0.183	0.256	0.217	-0.136	-0.049	**0.377**	**0.371**	**0.380**
Computer Application - Others	-0.035	-0.197	-0.030	-0.147	-0.188	-0.022	-0.006	-0.040	-0.053	-0.073
Information Automation - Data Capture	0.279	**0.451**	**0.535**	**0.362**	0.267	**0.530**	**0.484**	0.117	**0.449**	**0.497**
Information Automation - Data Download	0.329	**0.591**	**0.737**	**0.568**	**0.459**	**0.508**	**0.443**	0.260	**0.482**	**0.466**
Information Automation - Monitoring	**0.588**	**0.568**	0.178	**0.515**	0.176	**0.371**	0.219	0.082	**0.566**	**0.490**
Material Handling Automation - Step	0.278	**0.419**	**0.608**	**0.602**	**0.471**	**0.464**	**0.430**	**0.630**	0.339	**0.379**
Material Handling Automation - IntraBay	0.175	-0.066	0.279	0.221	**0.357**	0.091	0.121	0.279	0.192	0.294
Material Handling Automation - InterBay	**0.644**	**0.455**	0.303	**0.743**	0.297	**0.455**	0.325	0.104	**0.692**	**0.435**

Table 3.6.5 Correlations of CIM and Automation Practices with Performance - All Fabs

COMPUTERIZED APPLICATIONS	Defect density	Line yield	Stpr tput	Imp tput	Met tput	DL prod	TL prod	Cycle time	Integ yield	Integ stpr tput
Lot Operations										
WIP tracking	0.085	**0.526**	**0.522**	0.344	0.295	**0.435**	0.331	0.044	**0.492**	**0.396**
Recipe management	0.180	0.330	0.241	**0.397**	0.323	0.038	0.083	**0.428**	**0.437**	0.141
Reticle tracking and verification	0.230	0.107	0.291	**0.465**	**0.482**	0.165	0.108	0.201	**0.388**	0.340
Bay or block controller	-0.076	0.165	**0.398**	0.312	0.148	0.270	0.313	0.100	0.072	-0.054
Equipment & Process Tracking										
Equipment tracking	-0.128	-0.281	0.016	-0.349	-0.173	0.005	0.136	-0.011	-0.264	-0.143
Engineering Data Collection	0.137	**0.484**	0.029	**0.405**	0.246	-0.117	-0.123	0.150	-0.013	0.111
Statistical Process Control	-0.071	-0.027	0.278	-0.204	0.026	0.185	0.246	-0.020	0.064	-0.092
Trouble-shooting assistance	-0.103	0.213	0.232	0.104	0.148	0.307	0.334	**0.450**	0.110	0.007
In-line wafer maps	0.151	0.027	-0.456	0.004	-0.280	-0.097	-0.157	-0.161	0.107	-0.073
Scheduling										
On-line lot scheduling	-0.448	-0.526	-0.088	-0.321	-0.004	-0.378	-0.273	-0.102	-0.227	-0.504
Kanban	-0.103	0.117	0.232	0.204	0.250	0.097	0.228	0.016	-0.044	-0.191
Preventive maintenance scheduling	0.184	-0.267	NA	-0.196	-0.156	0.202	0.228	-0.092	NA	0.106
Shift scheduling - fab wide	-0.177	-0.160	0.107	-0.244	-0.052	-0.019	0.098	-0.080	-0.209	-0.037
Shift scheduling - fab start only	-0.270	0.015	-0.016	-0.205	-0.108	-0.151	-0.136	-0.290	-0.198	-0.132
Production planning	-0.302	-0.349	-0.056	-0.171	-0.191	-0.102	-0.026	0.211	-0.308	-0.228
Capacity planning	0.071	0.267	0.078	-0.120	0.059	-0.010	0.020	**0.382**	0.013	0.340
Fab simulation	0.128	0.281	-0.016	-0.067	0.032	0.140	0.158	0.312	0.110	0.280
Yield Analysis										
End of line wafer maps & bit maps	**0.558**	**0.380**	0.057	**0.581**	0.323	0.056	0.034	0.246	**0.420**	**0.361**
Integrated prod'n, EDC, & yield DB	**0.562**	**0.417**	-0.025	**0.527**	0.325	0.054	0.004	**0.353**	**0.428**	**0.506**
Relational database for analysis	-0.101	-0.160	-0.454	-0.255	-0.089	-0.448	-0.289	0.170	-0.087	0.025
Stat analysis of yield vs. in-line data	**0.466**	**0.349**	-0.197	**0.435**	0.072	-0.097	-0.173	-0.083	**0.364**	**0.465**
Stat tools connected to analysis DB	0.151	0.063	-0.184	-0.110	-0.108	-0.118	-0.049	**0.360**	0.063	0.191
Statistical analysis reports	0.312	-0.075	0.231	0.130	0.041	0.142	0.263	0.150	0.301	0.190
Ad-hoc query capability for analysis	-0.152	-0.108	-0.154	-0.168	0.076	-0.167	-0.004	**0.402**	0.067	-0.082
Others										
Materials purchasing & order tracking	-0.236	-0.118	0.179	-0.054	-0.092	0.053	-0.020	-0.314	-0.087	-0.264
Computerized doc control systems	0.311	0.101	0.060	-0.095	0.219	-0.013	0.027	0.173	0.072	**0.347**
Costing & financial valuations	-0.072	-0.295	-0.284	-0.131	-0.299	-0.079	-0.010	0.105	-0.070	-0.137

Table 3.6.5 Correlations of CIM and Automation Practices with Performance - All Fabs (cont.)

	Defect density	Line yield	Stpr tput	Imp tput	Met tput	DL prod	TL prod	Cycle time	Integ yield	Integ stpr tput
INFORMATION AUTOMATION										
Data Capture										
Auto-upload metrology data	0.325	0.326	0.252	**0.364**	0.296	0.225	0.171	-0.019	0.006	**0.354**
Auto-upload process EDC	0.158	**0.462**	**0.580**	0.235	0.224	**0.527**	**0.447**	0.192	**0.367**	**0.394**
Auto SPC data entry	0.091	0.219	**0.476**	0.145	0.265	0.147	0.201	0.230	0.099	**0.348**
Auto-upload in-line elec test results	0.267	0.117	-0.028	0.125	0.153	0.041	0.070	0.019	0.246	0.151
Auto-upload sample probe results	0.060	0.102	0.104	0.080	-0.006	0.143	0.258	-0.136	-0.064	0.230
Auto WIP tracking data entry	-0.025	0.048	**0.516**	0.234	0.080	**0.414**	0.287	0.073	**0.368**	0.069
Auto equipment tracking	0.156	0.256	0.298	0.173	0.123	**0.391**	**0.457**	0.240	**0.432**	0.330
Auto equip. tracking data entry	0.286	**0.615**	**0.451**	**0.417**	0.170	**0.516**	**0.420**	0.220	**0.659**	**0.562**
Auto metrology equip. status upload	0.280	0.309	0.232	0.104	0.047	**0.412**	0.334	-0.201	**0.383**	0.305
Data Download										
Auto-recipe download	0.171	**0.541**	**0.712**	**0.390**	**0.336**	**0.399**	**0.438**	**0.388**	0.332	**0.386**
Auto sanity-check machine <-> lot	**0.386**	**0.503**	**0.580**	**0.583**	**0.403**	**0.486**	**0.350**	0.098	**0.487**	**0.430**
Monitoring										
Process out of control alarms	**0.413**	0.173	-0.035	0.154	0.069	0.143	0.023	0.024	**0.406**	0.230
Machine trouble or idle alarms	**0.528**	**0.714**	0.302	**0.648**	0.162	**0.440**	0.315	0.105	**0.485**	**0.543**
MATERIAL HANDLING AUTOMATION										
Step Automation										
SMIF	0.129	-0.020	-0.028	0.098	0.299	-0.160	-0.083	0.123	0.031	0.199
All machines robot load/unload	0.202	**0.414**	**0.624**	**0.557**	**0.522**	**0.415**	**0.387**	**0.571**	0.295	**0.387**
Wet bench robot	0.029	**0.421**	0.281	**0.435**	0.232	**0.374**	0.325	0.288	**0.407**	0.091
Linked or robotic lithography	**0.408**	0.267	**0.536**	**0.650**	**0.573**	**0.389**	**0.393**	**0.462**	0.318	**0.514**
Diffusion furnace robot	0.042	0.331	0.265	0.160	0.089	0.109	0.096	**0.488**	-0.124	0.075
Other deposition area robot	0.071	0.027	**0.487**	0.214	-0.026	**0.515**	**0.462**	0.291	0.264	0.009
Etch area robot	0.261	0.281	0.336	**0.349**	0.032	0.286	0.158	0.312	0.264	0.280
Intrabay Automation										
Auto-locate lot and reticle	-0.005	0.148	0.336	0.072	0.314	0.140	0.158	0.162	0.110	0.280
Auto reticle retrieval and storage	0.234	-0.222	0.058	0.224	0.172	-0.007	0.015	0.220	0.151	0.132
Interbay Automation										
RR and stockers	**0.528**	**0.490**	0.258	**0.480**	**0.060**	**0.440**	**0.350**	0.032	**0.485**	**0.345**
AGVs and stockers	0.280	0.021	0.104	**0.505**	**0.351**	0.097	0.016	0.125	**0.383**	0.206

Note: NA - not available

Table 3.6.6 Correlations Between CIM and Automation Practice Areas

	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11
Computer Application - Lot Operations (X1)	1.000	0.026	0.111	0.482	-0.152	0.529	0.697	0.161	0.519	0.456	0.510
Computer Application - Eqpt Tracking (X2)		1.000	0.044	0.299	0.224	0.310	0.172	0.165	0.145	0.132	0.212
Computer Application - Scheduling (X3)			1.000	0.109	-0.048	0.021	-0.027	-0.556	-0.091	0.321	-0.454
Computer Application - Yield Analysis (X4)				1.000	0.013	0.200	0.204	0.253	0.213	0.519	0.263
Computer Application - Others (X5)					1.000	-0.044	-0.222	0.205	0.009	-0.202	-0.094
Information Automation - Data Capture (X6)						1.000	0.821	0.325	0.448	0.261	0.559
Information Automation - Data Download (X7)							1.000	0.308	0.506	0.309	0.619
Information Automation - Monitoring (X8)								1.000	0.308	-0.226	0.648
Material Handling Automation - Step (X9)									1.000	0.197	0.285
Material Handling Automation - IntraBay (X10)										1.000	0.192
Material Handling Automation - InterBay (X11)											1.000

3.7. On-Time Delivery
by Veronica Bixuan Wu

As semiconductor manufacturing matures, the importance of on-time delivery has grown in many companies. Short customer lead times and accurate fulfillment of delivery promises are now critical to the competitiveness of many companies. In this study, the ability to commit to a delivery schedule and subsequently meet the commitment is what we term *on-time delivery.*

While it is difficult to express a detailed prescription for on-time delivery, the essential foundation upon which superior on-time delivery performance can be built is the coordination of the efforts of various functions, from marketing to production planning to manufacturing. The sales and marketing groups in a semiconductor company has responsibility for forecasting future demands as well as for providing delivery quotations in response to customer inquiries for products. Manufacturing is responsible for providing statements of available production capacity as well as for the management of the production process to achieve production targets. The function of production planning is to merge the information from both marketing and manufacturing and provide volume and mix decisions.

In this section, we examine the on-time delivery performance and production planning systems as they relate to the wafer fab portion of the manufacturing process. The role of the sales and marketing functions is beyond the scope of this study. Many of the manufacturing aspects which impact on time-delivery such as yield and cycle time are discussed elsewhere in this report.

Examining on-time delivery and production planning from the wafer fab perspective has advantages as well as drawbacks. Although on the surface, fab delivery performance does not appear to directly impact a customer who purchases packaged chips as finished goods, the time-consuming manufacturing process in the fab is the longest and most uncertain portion in the manufacture of packaged semiconductors. Consequently, the delivery performance of the fab can be viewed as an key indicator of the overall delivery performance, unless cycle time buffers are added in the assembly process or large inventories are kept either after wafer probe or at finished goods. Both of these options are undesirable from an operational efficiency standpoint. In addition, due to not uncommon large errors in forecasting, large inventories can be a tremendous economic burden when products become obsolete.

Production planning at many semiconductor companies is centrally run, which means that there is a company-wide or site-wide planning organization which takes responsibility for much of the planning activities. Since our site visit is usually limited to discussions with representatives of a specific fab, most times we did not have an opportunity to speak to a representative of this planning group. However, the fab representatives typically are sufficiently informed about central planning so that we can get the idea of the functions performed there. In all likelihood, we lose some information about the overall planning process when visiting a fab of a company with a central planning group. On the other hand, we gain the ability to study in depth what data the fabs collect and use for planning purposes. As we will explore later, the use of fab data plays a key role in the effectiveness of production planning.

On-Time Delivery Measurement and Performance

After visiting almost thirty fabs producing a variety of product types in the semiconductor business, it became clear that there is not one standard which fabs use to measure on-time delivery. In fact, one of the fabs which we visited did not begin to formally to measure on-time delivery until a few months before our visit. Some of the differences in measurement effort may be attributed to the type of products which the fab manufactures and the planning methodology which the fab uses (to be discussed later in this section). For instance, one of the fabs had a fixed production schedule dictated by central planning, and the fab was not allowed to change this plan. They measured their on-time delivery as the ratio of actual output to the planned output. This fab, and several others with this sort of internal performance metric, responded to our mail-out questionnaire with an on-time delivery performance in some months exceeding 100%, which was puzzling to us until the meeting with them.

Some companies use more than one metric to measure on-time delivery, and some measure delivery performance at multiple points in the overall process, such as at fab out, at probe out, at die received at assembly plant, at customer shipment, etc. Having more than one measurement point is helpful to companies for pinpointing their problem areas and focusing their attention.

Among the variety of metrics used for on-time delivery, there are a few metrics used more frequently and widely than others. These include line item performance and volume line item performance. Such metrics were discussed in our previous report, [23] so they won't be explained here.

There are several fabs we visited who have been quite innovative in on-time delivery measurement, and they have devised metrics which we consider superior to the metrics in more general use. One of these fabs uses a *linearity* score, which compares each day's actual die output to the planned output, and also compares the cumulated output month to date to the cumulated planned output to date. The end of the month score for the fab is the average of each day's score. The maximum score is one, which means that overproduction does not earn credit. This score intrinsically emphasizes the idea of smooth production and timeliness of production at the same time, unlike other measures which only account for the delivery of the item, regardless of the production flow.

Of course, superior metrics do not automatically translate into superior manufacturing performance. Almost any of the metrics we encountered can be informative if used correctly, although one might give more information than another. The key factor is the organization's effort to analyze for cause their metric scores and to learn from them.

The range of the reported on-time delivery scores for the fabs in our study varies from a low 30% to a high of 100%. This range demonstrates that, even when judged by their own metrics, some fabs perform poorly with respect to others whose standards for performance may be more stringent. For the poor-performing fabs, it is not unusual to observe large fluctuations in on-time delivery over consecutive months.

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23. "On Time Delivery Improvement," by Robert F. Benson, in *The Competitive Semiconductor Manufacturing Survey: Second Report on Results of the Main Phase,* R. C. Leachman (ed.), Report CSM-08, Engineering Systems Research Center, Univ. of Calif. at Berkeley, Berkeley, CA 94720 (Sept. 1994).

In contrast, top delivery performers display consistency in on-time delivery performance. The top performers tend to have (1) a low workload relative to capacity (such as for end-of-life fabs), (2) an effective planning system incorporating good capacity analysis, (3) a stable manufacturing process, (4) time buffers added on top of the mean factory cycle time that are used to pad delivery dates, (5) planning yields set a lower levels than mean yields, or some combination of these five factors.

An essential element common to most top performers in delivery, we discovered, is the use of high-quality planning models incorporating good capacity analysis constructed by the fabs. Cycle time padding can promote improved delivery performance, but it is not as effective, since fabs emphasizing padding tend to be imprecise in their estimates of capacity and other production parameters. As we observed, when fabs try to be precise, they are able to use data which they collect more effectively, leading to a better understanding of their production process and consequent productivity improvements.

Good cycle time and yield performances tend to be relatively good indicators of on-time delivery performance, although not absolute. While it remains difficult for fabs to trade off aggressive commitments and good metric scores, it is always beneficial for them to pursue improvements in both at the same time. One mistake which many fabs make is focus only on improvement of one or a few aspects of manufacturing. This is the reason why some fabs perform better in one category and worse in others. A more balanced approach should be taken. Due to the requirement to involve many functions, the a strong production planning system can be very conducive to such a strategy.

Production Planning

Production planning methodology employed by the fabs in our survey varies drastically. Most of the fabs use internally-developed, proprietary software for their planning calculations, rather than commercial software. The complexity and sophistication of these software covers a wide range, from simplistic spreadsheet calculations to mathematical optimization and artificial intelligence heuristics. At one end of the spectrum, we have seen fully automated, fully integrated planning systems which take cycle time, equipment capacity, yields and process route data to produce a complete production plan from fab starts to finished goods shipment. Then there are fabs who rely on numerous software applications, each responsible for a part of the planning stage, whereby the output of one application must be fed into others. Spreadsheets are used in about half of the participants when calculating the fab start schedules. Many of the fabs receive proposed planning schedules calculated by a central group, analyze the proposals, and provide a response to adjust for the final commit schedule. Only a few fabs are totally not involved in scheduling and produce exactly according to a centrally calculated plan.

Both the *planning cycle time,* which is the time required to generate a complete production plan, and the planning frequency differ among our participants by an order of magnitude. We have seen planning cycle times anywhere from several hours to several weeks. Planning frequency ranges from daily to semiannually. When an automated planning software is used, and all the required data are collected in a timely fashion, the planning cycle time tends to be short. In contrast, at fabs who do not maintain good databases for the purposes of planning and at companies without a comprehensive software, there is a lot more back-and-forth between the fab and

the central planners, resulting in a prolonged planning cycle time. The longer planning cycle time means a lower planning frequency. When the planning cycle time is reduced, the fab may then adjust its plan and respond to changes in the marketplace or the manufacturing environment much more quickly. Some fabs use *incremental planning* as a way to reduce the planning cycle time and provide increased responsiveness. Rather than re-plan all products in batch mode, new demands are loaded onto the factory on a first-come, first-serve basis according to unreserved and available capacity. This approach can be especially beneficial to the ASIC manufacturers, since it allows them to quickly revise the production plan and calculate availability for the customer.

One of the most fundamental elements of effective production planning is a fab's ability to estimate its production capability, also known as the capacity model. To establish a good capacity model, the fab must first have a good understanding of the process flows and almost all aspects of production. Poor capacity models may lead to overloading of the fab during transitions in the product mix, resulting in excessive WIP and poor on-time delivery or cycle time performance. For instance, some fabs define capacity simply as the maximum number of wafer starts per month, regardless of the mix. Worse than that, due to the lack of attention or lack of data analysis, some fabs actually have very little knowledge of what their real capacity is. So they use their judgement to manually estimate their capacity.

Incredibly, the most common capacity model we encounter is a simple upper bound on the aggregate number of wafer starts per week or per month, supplemented with conversion factors for products produced in different process flows. While the simplicity of such an approach may be appealing, on-time delivery is difficult to achieve while maintaining full production during changes in the process mix. The only fabs we have seen that consistently maintain delivery and cycle time performance under such conditions maintain a capacity model which encompasses careful measurements of the available time of key resource types such as machines, operators, reticles, etc. These fabs make a dynamic computation of the consumption of these resources along the production routes to make sure planned volumes do not overload any key resources. These fabs can promptly and accurately adjust for the changes in product mix and volume, since they measure resource consumption through time as products are planned to move along their process routes.

A capacity analysis requires accurate and effective data collection to support it. Typically, historical cycle times, processing rates and yields are used, to be applied to static data describing process flows, to status data such as work-in-process levels, and to dynamic data describing demands received from marketing or sales. The accuracy of these data among our participants may may vary over a quite large range. There are still fabs which manually enter these data into spreadsheets, and many data are often estimates rather than actual measurements. The most advanced fabs develop automated data collection systems to gather data on their scarce resources, insuring accuracy and timeliness of the data. This may well be the most crucial steps in all of production planning. One fab manager we interviewed noted that "developing the management of data was much more of a challenge than creating the software."

The level of detail and the time horizon of production planning is another distinguishing feature of our participants. Some companies make a very long term strategic plan, one as far out as five years, then a tactical or operational plan which is of shorter horizon. The monthly or weekly production plans are then produced following these guidelines. The level of detail in the

production plan ranges from daily to weekly to monthly time buckets.

Almost all fabs use some kind of smoothing of production starts. It is not clear that a multi-level planning hierarchy means better planning. In fact, depending on how often the long term plans are updated, the hierarchy can actually impede production planning, since within the semiconductor industry it is very hard to predict future demands. This is another reason a strong and responsive planning system is necessary: errors in demand forecasting are prevalent and sometimes quite large.

As mentioned in our previous report, [24] the number of people who are involved in planning sometimes appears to be in inverse proportion to the effectiveness of production planning. Automated planning systems take a relatively small staff to maintain accurate data collection and execute the planning system, whereas the more manual planning approaches require many more staff from sales, marketing, engineering, and manufacturing to adjust, negotiate and replan. Even though more people are involved in the latter approach, the plans so generated tend to be of inferior quality.

The effort to develop and implement the automated planning system in use at one of our participants was awarded the Franz Edelman Prize, an annual award among international contestants for the best industrial application of management science. This participant routinely achieves 95% line item delivery performance in customer shipment across more than 8,000 finished goods types. [25]

Scheduling and Dispatching

While production planning is the strongest driving force behind on-time delivery performance, automated scheduling and dispatching systems are also helpful to insure production plans are executed successfully. Fabs which have automated data collection systems are much more likely to have automated scheduling and dispatching. Fabs which do not have automated scheduling systems are dependent on human judgement, such as direction from the shift leaders and supervisors, or the operator's own decision.

The overall scheduling function may be divided into (1) release of new production lots into the fab, and (2) dispatching or scheduling work-in-process (WIP) at each equipment bay in the fab. Although not really instructions for execution, another form of scheduling we encounter is the establishment of short-term goals for productivity by the entire fab or by individual process modules or equipment bays. We discuss each kind of scheduling below.

In general, release schedules are translated from the production plan by smoothing the plan. Some fabs use DGRs (daily going rates) to calculate their release schedule. In one top-performing fab with respect to on-time delivery, release scheduling is completed by using essentially the automated plan with maybe tiny adjustments. One of the managers reported that he uses 90% of the plan, and changes only 10% according to fab circumstances. Again, here we encounter the same problem as in planning. When no automated system exists, scheduling becomes personal

24. Benson, Robert F. [1994], *op. cit.*

25. See "IMPReSS: An Automated Production Planning and Delivery Quotation System at Harris Corporation - Semiconductor Sector," by R. C. Leachman, R. F. Benson, C. Liu and D. J. Raar, *Interfaces,* **26** (1), p. 6-37 (Jan - Feb, 1996).

judgement.

Fab-wide productivity goals most commonly are expressed as a targeted number of wafer "moves" per shift or day, and sometimes as a targeted number of lots processed per shift and/or day.

Fabs use different rules for dispatching. Simple dispatching rules such as FIFO, with exceptions made for rushed or hot lots, are used by quite a few fabs. A dispatching rule common at ASIC fabs is *due date dispatching* or *critical ratio dispatching*. Using the former rule, the expected date out of the fab for a lot (based on planned cycle time) is subtracted from the scheduled due date, and the lot with the lowest score (the "least slack") is processed first. Using the latter rule, a ratio is computed of the expected date out of the fab for a lot divided by the scheduled due date. The larger the number, the higher the priority.

About 25% of the fabs we visited also apply some sort of Kanban rules for controlling the dispatching in order to keep WIP in check. These rules inhibit selection of certain lots if downstream WIP in the particular process flow is excessive.

About half of the fabs we visited have automated their dispatching system, so that operators can consult with the computer or other video display for advice on which lot to process next. Hardly any such fabs require strict enforcement of the computer's recommendation. In one fab, one operator responded that he hardly uses the computer. In contrast, some fabs make strict enforcement. One fab has automated the system so that the WIP rack is electronically connected to the computer. When an operator needs to process the next lot, a green light will flash at the position where that lot is located on the rack. If an operator takes a wrong lot, a red light will blink and the machine will refuse to process. Some of these features are discussed in the Section 3.6 (CIM and Automation Practices), but to the extent that this company has strictly enforced its dispatching rules, we find it praise-worthy.

Summary

The additional visits to twelve more fabs since last report have enabled us to see more variety in the practices within the industry. We are excited by the innovation of various fabs. They reinforce in our minds the advantages of automation in production planning. The different metrics used by the fabs made it more difficult to compare their on-time delivery performance. However, a closer look at the different planning methodologies provided insights to some of the underlying concerns on which fabs should start to focus.

The most critical factor for on-time delivery improvement continues to be the company's dedication and focus on the production planning problem. We have found that most participating companies, once they set their mind to improving something, were able to succeed. So management effort and cooperation within the company is still the ultimate factor. Improving production planning practice is a major challenge since it touches almost all departments of a company. Major improvements in data collection systems and in data maintenance are required. Overcoming the resistance encountered when change in management culture is undertaken remains the greatest challenge.

3.8. Human Resource Practices
by Clair Brown

This section on human resource (HR) practices summarizes our preliminary findings from the HR section of the mail-out questionnaire (MOQ). The HR section of the MOQ covers the main components of a fab's human resource system: Hiring and lay offs (quantity); Internal allocation of labor (job assignment, promotion, shift schedule, overtime); Work organization (work process, teams, functional divisions) and communication structures; Training and skill development (quality); Compensation and evaluation; and Division of tasks (across occupations) and career ladders. We have collected and analyzed the responses from fifteen fabs on three continents.

A more complete compilation of our findings can be found in "The Competitive Semiconductor Manufacturing Human Resources Project: Second Interim Report," Clair Brown, ed., Report CSM-32, Institute of Industrial Relations, University of California at Berkeley, 2521 Channing Way, Berkeley, CA 94720 (July, 1996). That report also summarizes the findings of several HR focus studies. These findings include preliminary results from on-going studies on the transferability of HR practices, on the evolution of skills and careers at one major U.S. company, on inter-firm knowledge sharing, and on managing creativity and control in innovation, as well as the findings of completed focus studies on a statistical analysis of the initial interview data and a comparison of these data with a subset of responses to the HR questionnaire, on team organization and process, and on human capital investment in learning-by-doing.

The CSM-HR group is led by Prof. Clair Brown and includes Prof. Michael Reich and graduate students Melissa Appleyard, Jumbi Edulbehram, Dan Rascher, and Vince Valvano. Past members have included postdoctoral fellow David Bowen, and the late Adjunct Professor Vinay Sohoni. We have been very fortunate to have collaborated in the past with graduate students Diane Bailey, Nile Hatch, Baruch Saeed, and Linda Sattler from the CSM main study.

Preliminary Conclusions

Our preliminary results confirm the main conclusion reported in the last report: [26] *High performing fabs have a human resource system with integrated, consistent parts and the system will be tailored to function in a specific environment.*

We find that successful systems not only include a seamless interplay of internal resources, but they also encourage the identification and incorporation of appropriate external knowledge and know-how. The effectiveness of any particular system will depend on its environment--the product market, the economic conditions, and the institutional and cultural system in which the company operates.

One must not analyze the relationship of a particular practice and firm performance only in isolation, since how a particular practice functions within the HR systems determines the relationship. For this reason, the CSM-HR team starts with the premise that "best practice" can take

26. *The Competitive Semiconductor Manufacturing Human Resources Project: First Interim Report,* Clair Brown, ed., Report CSM-09, Institute of Industrial Relations, University of California at Berkeley, 2521 Channing Way, Berkeley, CA 94720 (September, 1994).

more than one path. One set of "best practices" does not necessarily exist for all environments. In fact, more than one HR system may perform well in any particular set of circumstances, since trade-offs may exist between the component parts of a system. However, not all HR systems are internally consistent, and not all HR systems function equally well. In the former case, firms may inadvertently create "hybrids" that use incompatible components and result in unintended consequences. In the latter case, some HR systems may not adapt adequately or rapidly enough to changes in the environment or management may attempt to import one innovation in HR practices without ensuring that other changes are made to keep the system integrated and consistent.

Analysis of Responses to the Mail-Out Questionnaire

Our initial HR analysis, which relied upon interviews with a few non-randomly chosen employees (operators, technicians, supervisors, and engineers) , found some intriguing results, which we compared to our findings from the questionnaire. However, we did not know how representative these employee responses were, and to what extent their personal experience could be used to document the participants' HR systems. Also, these variables were not collected as a systematic documentation of the HR system, and therefore they did not necessarily provide information on the systematic linkages among the parts of the HR (or employment) system of the firm. We used these preliminary results as a guide in developing a more systematic and comprehensive questionnaire on employment and training practices. The HR section of the CSM survey Mail-Out Questionnaire (MOQ) was expanded to include this questionnaire. This expanded HR section of the MOQ was sent to previous participants, and became a regular section of the MOQ for participants joining the survey since our last report. [27] We received completed HR questionnaires from only three of the previous 16 participants. Combining these three with the responses received from the 12 participants joining the CSM survey since our last report, our analysis is thus based on data collected from 15 fabs.

We have relied on our understanding gained in our fieldwork rather than strictly on statistical significance in presenting our findings. Because of the rich set of performance metrics available, whenever possible, the authors have paid attention to how practices affect specific outcomes, such as defect density, line yield, cycle time, labor productivity, and these are presented in the findings. In this summary, however, patterns observed at the high performing fabs are usually mentioned without reference to particular performance metrics.

Innovative Human Resource Policies

Systematic differences in practices exist across fabs when they are grouped according to their major process flows (memory or logic) or according to region (Asia or the U.S.). Because most of the memory fabs in our sample are in Asia (4 of 5 fabs), it is not easy to distinguish between region-practice and process-practice correlations. For this reason, observed differences cannot always be related to the institutional structure or to the product type, since both of the attributes are important in defining the environment.

27. Brown, Clair (ed.) [1994], *op. cit.*

Logic (and U.S.) fabs are more likely to use a variety of team structures (cross-functional, self-directed work teams, and quality improvement). Memory (and Asian) fabs tend to restrict their teams to quality improvement efforts. Our site visits gave no indication that the number or variety of teams in place at a fab is positively related to the amount and quality of problem-solving activity. American fabs tend to have a shorter track record with team organization and may be trying to learn what types of teams work best. Asian fabs use a wider range of compensation policies than logic fabs. Suggestion and knowledge pay policies are also more prevalent.

Work organization differs significantly across fabs by region. Shift rotation for operators is widespread in Asia (but not the U.S.) Job rotation for engineers is also the norm in Asian fabs. Moreover, in U.S. fabs, operator job rotation is not a common practice, unlike in the Asian fabs.

Employment and Turnover

Between 1990-1994, employment levels were more stable in the U.S. than in the Asian fabs. The Asian fabs have more turnover (mostly quits) than the U.S. fabs, and this reflects the use of female operators who leave the work force early to start families as well as the local competition for workers. One example of a less stable work situation comes from one fab, which is trying to decrease its headcount by 40% while it doubles its productivity.

Asian fabs have more workers of all types than U.S. fabs in our sample, reflecting the larger average size of the Asian (memory) fabs. In general, memory fabs have more operators but fewer engineers than logic fabs. There is a higher ratio of equipment to process technicians than equipment to process engineers because of the cleaning and maintenance activities performed by technicians. On the other hand, engineers are the primary workers involved in process design, implementation, and testing.

Logic chip manufacturing uses more engineers, supervisors, and managers per operator and technician than memory chip production. In the U.S., logic producers use fewer engineers than Asian logic manufacturers per total employees. A higher number of operators per supervisor is associated with lower performances in defect density and direct labor productivity. A high ratio of operators per engineer is correlated with higher defect densities and higher stepper throughput.

Career Ladders

There is significant variation in employee experience levels in our sample of semiconductor fabs. One-third of our sample fabs had experienced operator work forces such that at least half or more of operators had five or more years of tenure. At several fabs, however, a majority of operators had less than two years of tenure. Majority-female operator work forces are common in semiconductor fabs and predominate in our sample. The engineering work forces in our sample had higher levels of fab tenure than operators. Most fabs reported that a majority of their engineers had at least five years of tenure.

We find a significant degree of wage-level dispersion across our sample fabs. This is expected given that the sample fabs span six countries and three continents. Most fabs in our sample reported operator career ladders with four grades and fairly flat wage paths across grades. Career ladders for technicians exhibit more steepness than those for operators. Engineer career ladders are longer and the wage paths more steeply sloped, relative to those for operators and

technicians.

In our sample, we do not observe a positive relation between work force experience and wage path steepness, as might be expected if a principal goal of career ladders is to retain experienced employees.

Job assignments may or may not translate into job ladders. This relationship depends on the use of job assignment to achieve skill acquisition (i.e., learning a new task and multi-skilling) or achieve skill deepening (i.e., learning how to solve problems or make repairs) or reward workers with a preferred assignment. Job assignment may be used by management as a strategy for developing skills, or job assignment may be used by employees to improve their own working conditions. Similarly, job rotation may or may not be part of a system of multi-skilling and flexibility; instead, it may be part of a system of job control to relieve monotony or to decrease injuries. In the high performing fabs, we observed that job assignments were an integral part of the training process and were used both to broaden and deepen skills and well as to reward for good performance.

Appraisal and Promotion

We asked the fabs to rank the following criteria in order of importance for promotion: Attendance, Attitude, Output or Work Goals, Quality Record, Skill Level, Number of Skills, Team Participation, and Tenure. Given the technical complexity of each step of the semiconductor process flow and the need to understand these complexities for effective trouble-shooting, the data show that fabs value skill depth more highly than skill breadth. Of the eight performance criteria, the fabrication plants in our sample ranked Skill Level at the top for all job categories--engineers, operators, and technicians. Number of Skills, our proxy for skill breadth, ranked no higher than fifth.

Of the performance criteria, Tenure ranked last. Less than half the fabs in our sample even consider Tenure in promotion decisions. However, tenure and skill development are often closely related for operators and technicians, and so promotion based upon skill would result in similar outcomes to promotion based upon tenure with some exceptions at the high and low ends of performance and ability.

Few operators and technicians are ever promoted to other job categories. Only three fabs reported promoting more than ten operators to group leader, supervisor or technician. No fab reported promoting more than four technicians to a supervisor or engineer position. The limited number of promotions of operators and technicians outside of their job categories indicates that barriers exist. During site visits, we found that the primary barrier is additional schooling.

Another reason why few operators are promoted to the technician job category is cultural. A few fabs in our sample have barriers along gender lines: women are operators and men are technicians or engineers. A final reason for the limited mobility of hourly workers is a monetary reward issue. Some operators and technicians whom we met during our site visits said that they are reluctant to relinquish the ability to earn overtime pay for a salaried position.

Training

In our previous report, [28] we found that the practice of relying on prior experience was not an effective method of obtaining skilled operators and technicians. This implied that much of the important learning for operators and technicians occurs on-the-job in a particular fab environment.

The average number of days of initial training is similar across job categories, ranging from 21 to 27 days. The number of days of initial training is positively correlated with performance for all three job categories.

About 40% of each worker's time is spent in on-the-job training during the first year of employment across all three job categories, with an additional 5-8% of their time spent in the classroom. No significant correlations were found between this training and performance. After the first year, approximately 15% of each workers time is spent in on-the-job training, with an additional 6-10% spent in the classroom. Again, no significant correlations were found between this amount of training and the performance metrics. The results show that the type of training and how it is delivered is important, rather than the time in training.

It appears that using OJT training alone isn't useful with respect to increasing performance. For operators and engineers, using only classroom training hinders the goal of high performance. Technicians respond positively to solely classroom training. There is a positive correlation between the use of both types of training and the performance metrics across all job categories.

Skills and Work Tasks

Rapid and thorough problem-solving is a critical activity in the semiconductor industry. The initial data collection allowed us to draw preliminary conclusions about the relationship between HR practices and performance:

* Superior performance is associated with high technical content in operators' job responsibilities. To more thoroughly investigate this relation, our new questionnaire explores the distribution of equipment PM and SPC responsibilities among operators, technicians and engineers.

* Many engineers thought that they should be devoting their time to long-term, yield improvement projects rather than "fire-fighting" on the production line. Our data show, however, that engineering involvement in sustaining the production line correlates with high fab performance. We are studying to what degree techs and operators can substitute for engineers when problems occur.

Examination of the participation of operators, technicians and engineers in equipment maintenance and statistical process control (SPC) activities indicates that these findings are partially substantiated. Teamwork is commonplace in the majority of fabs in our sample, and teams at different fabs share many characteristics. The structuring of work tasks and the participation of workers in specific activities seems to have a bigger impact on performance than the characteristics of teams.

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28. Brown, Clair (ed.) [1994], op. cit.

Equipment maintenance and statistical process control (SPC) activities analyzed exhibit a greater degree of variation in human resources practices across the fifteen fabs than do the data on teams. Both equipment maintenance and SPC are central to effective problem-solving in a fab. The correlations for SPC activities and performance support the hypothesis that fabs that engage in technical tasks most intensively should exhibit the highest performance. The involvement of operators in equipment maintenance activities is positively correlated to performance; however, the involvement of technicians and engineers is not. So the hypothesis that fabs which include their "front-line of defense," namely their operators and technicians, in equipment maintenance and SPC achieve a higher level of performance is only partially supported. A fab's need to solve problems quickly and permanently requires operators and technicians to identify problems immediately and then work with engineers to uncover root causes and implement lasting solutions. We will continue to document how this process is most effectively achieved.

Summary of Findings and Job Prospects

The semiconductor industry provides a lot of training across all occupations, from operators to engineers. This training is necessary because workers are involved in continuous problem-solving in and industry that is continually introducing new processes or new products and is continually automating. After an average of a month of initial training, workers are receiving training about half the work time during the first year with the bulk of the training on the job. In subsequent years, about one-quarter of the time is spent in training (Table 3.8.1).

Training of technicians is more likely to correlated with the performance metrics than training of operators and engineers. We believe that this reflects the importance of machine up-time in determining machine productivity and the large variation in actual machine up-time observed across fabs. Fabs also exhibited large variations in the involvement of employees in equipment maintenance activities (Figure 3.8.1).

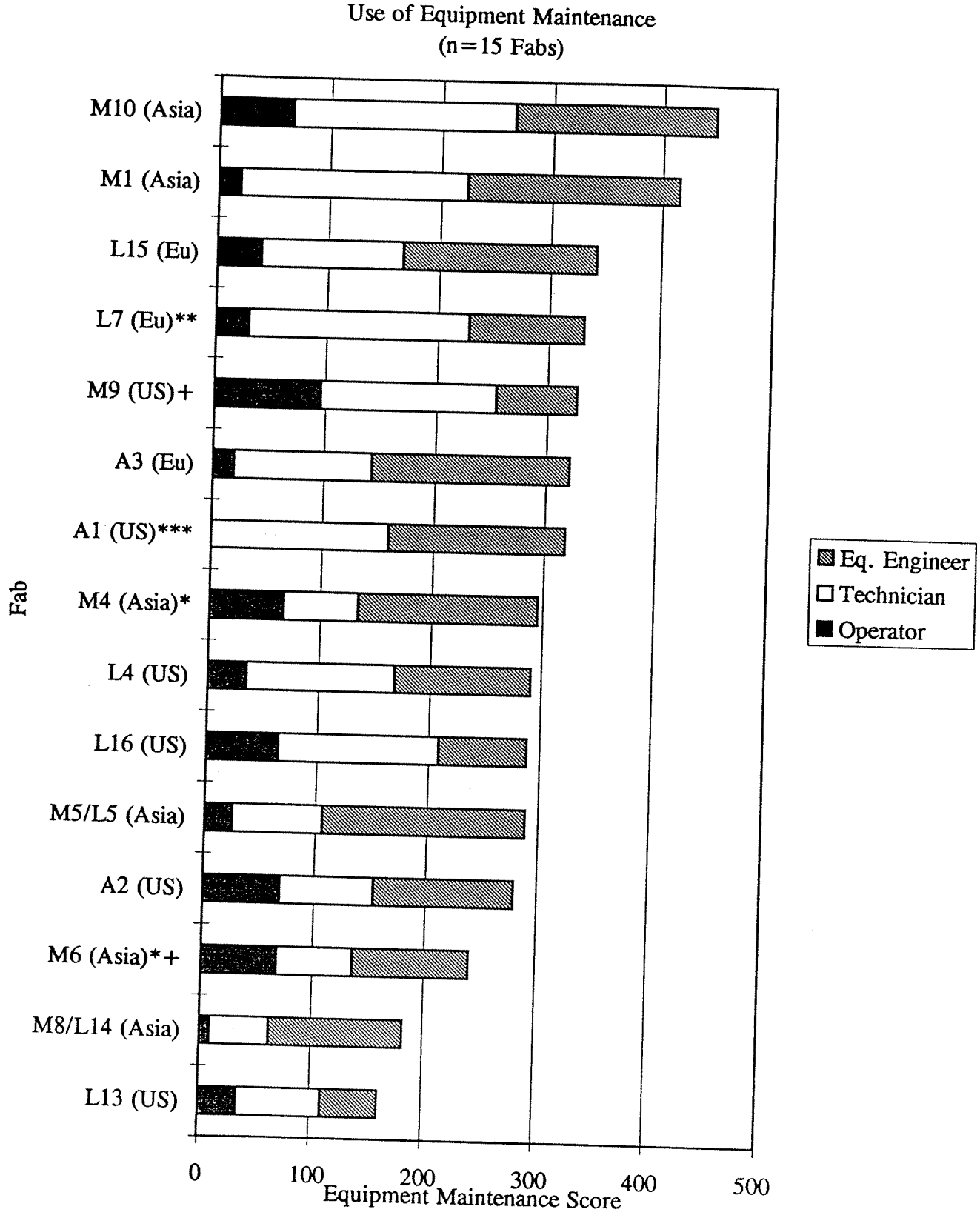
Operators are involved in fairly high skilled procedures, including various types of SPC (Figure 3.8.2) and equipment maintenance activities. Compared to operators in traditional manufacturing jobs, the operators in semiconductors oversee a highly technical process and undertake relatively complex technical tasks. Most operators are involved in data collection and monitoring, but the level of operator involvement declines as the difficulty of the task increases. The level of operator involvement in problem solving is usually limited to identify the nature of the problem and notify technicians or engineers. In a few fabs, operators are involved in performing some routine maintenance. Overall, operators perform tasks that require training and skill development. However, operators are still limited in their skill development and career growth, as well as wage growth, unless they become techs.

Two examples of career ladders for operator/technicians are shown in Table 3.8.2. All production workers in the large Japanese semiconductor companies are on a career ladder that combines operator and technician tasks, training and skills. By age 40, Japanese electronics workers have technical skills and job tasks. In the U.S., the operator jobs are usually separated from the technician jobs , and an operator does not necessarily (or usually) progress to a technician. However, most fabs provide the opportunity for an operator to move up to a technician job. To do this, the operator typically must return to school to earn an AA degree in electronics, since fewer than 10% of operators have AA degrees. They also must take some home study courses as well as

Table 3.8.1
Average Levels of Training Across Job Categories

	Orientation Initial Training (# Days)	First Year: Training or Learning New Skills (% of Time)		Subsequent Years: Training or Learning New Skills (% of Time)	
		OJT	Classroom	OJT	Classroom
Operators	27	40	5	16	6
Technicians	21	42	8	18	6
Engineers	26	39	8	12	10

Figure 3.8.1



*Operator scores were used for Technician scores, since one job category.
**Process Engineer scores used for Equipment Engineer scores, since latter not reported.
***Operator scores not reported.
+(Missing data for Equipment Engineer scores.)

Figure 3.8.2

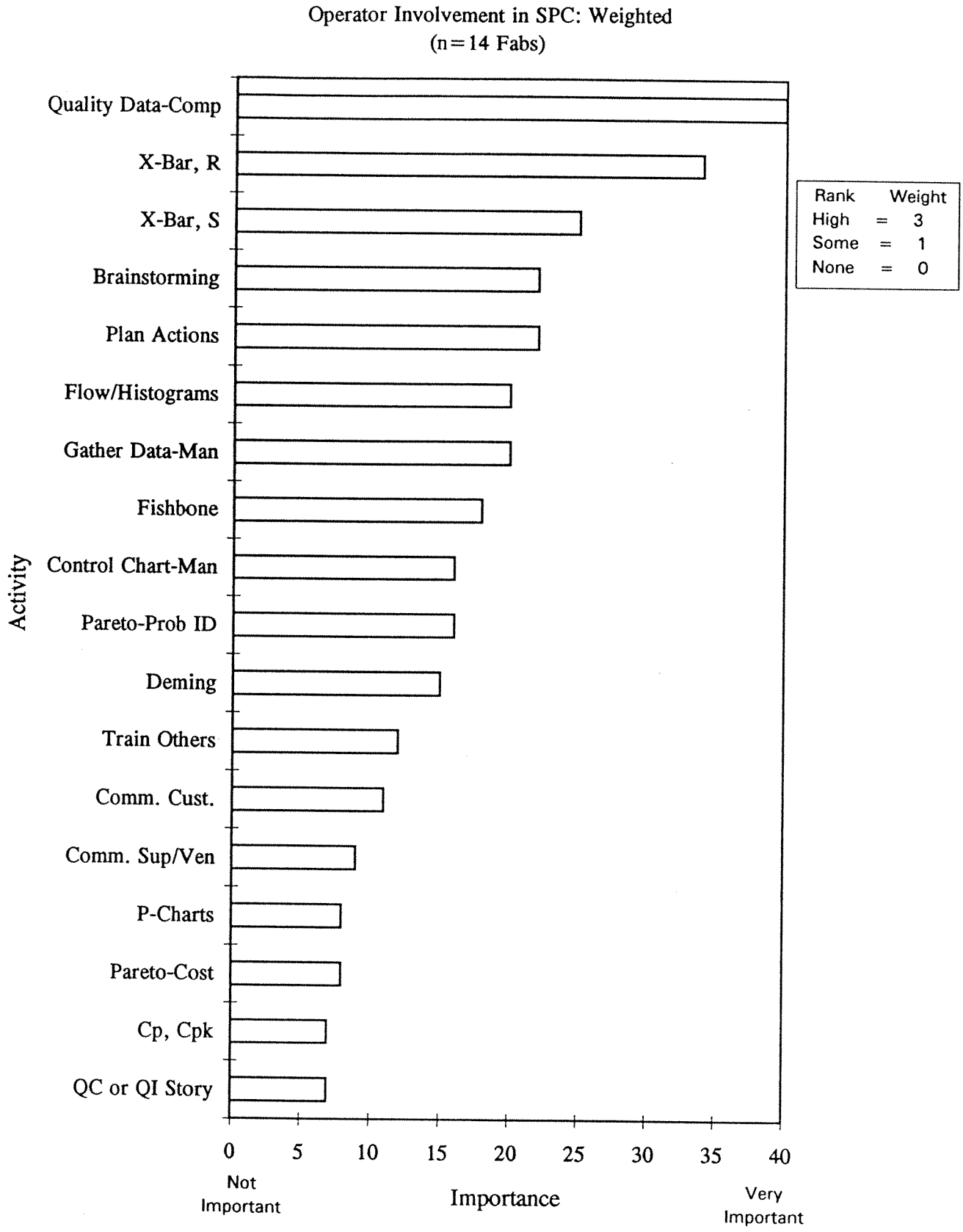

Operator Involvement in SPC: Weighted
(n=14 Fabs)
Quality Data-Comp
X-Bar, R
X-Bar, S
Brainstorming
Plan Actions
Flow/Histograms
Gather Data-Man
Fishbone
Control Chart-Man
Pareto-Prob ID
Deming
Train Others
Comm. Cust.
Comm. Sup/Ven
P-Charts
Pareto-Cost
Cp, Cpk
QC or QI Story
Activity
Rank Weight
High = 3
Some = 1
None = 0
0 5 10 15 20 25 30 35 40
Not Important
Importance
Very Important

Table 3.8.2
Examples of Career Ladders in Two Semiconductor Firms

U.S. Firm:

	Operator	Technician
Entry Wage	$7	$10
Top Wage	$15	$25
Top/Entry Pay Ratio	2.1	2.5
Approx. Time to Top	15 years	15 years

Japanese Firm:

	Operator
Entry Wage	893 ¥
Top Wage	3,201 ¥
Top/Entry Pay Ratio	3.6
Approx. Time to Top	20 + years

undertake specific company-provided training (including on the job training in certain processes.) The requirements are rigorous and require a lot of nonpaid time and commitment. At the U.S. company shown in the example, which encourages internal promotion, only one-third of the operators become technicians and one-half of the technicians were promoted from operator. For those operators who do become technicians at this U.S. company, their career ladders looks like the Japanese career ladder, which takes about 20 plus years and includes wages increasing 3.6 times.

Korean fabs provide an interesting contrast to both the Japanese and U.S. cases, since operator jobs are strictly segmented from technician jobs. Women, who live and work at the company for only three to five years before quitting to get married, are operators; men, who usually have long careers with the company, are technicians (as well as engineers and managers.)

Hourly earnings in the semiconductor industry have increased as the importance of technicians has increased (Figure 3.8.3). However, average earnings ($14.50) are still low compared to unionized production and craft workers. [29]

American companies increased employment in the U.S. relative to employment offshore since 1991, so that U.S. employment exceeded offshore employment in 1994 (Figure 3.8.4). [30] Overall, the outlook for employment, especially technicians and engineers, is strong even in the presence of continual automation. Although there is the potential for long career ladders for non-college graduates, the upgrading requires a technical education pursued outside of work as well as work-based training. The semiconductor industry pays relatively lower wages than unionized manufacturing but above average wages for all manufacturing, which has lower skill requirements.

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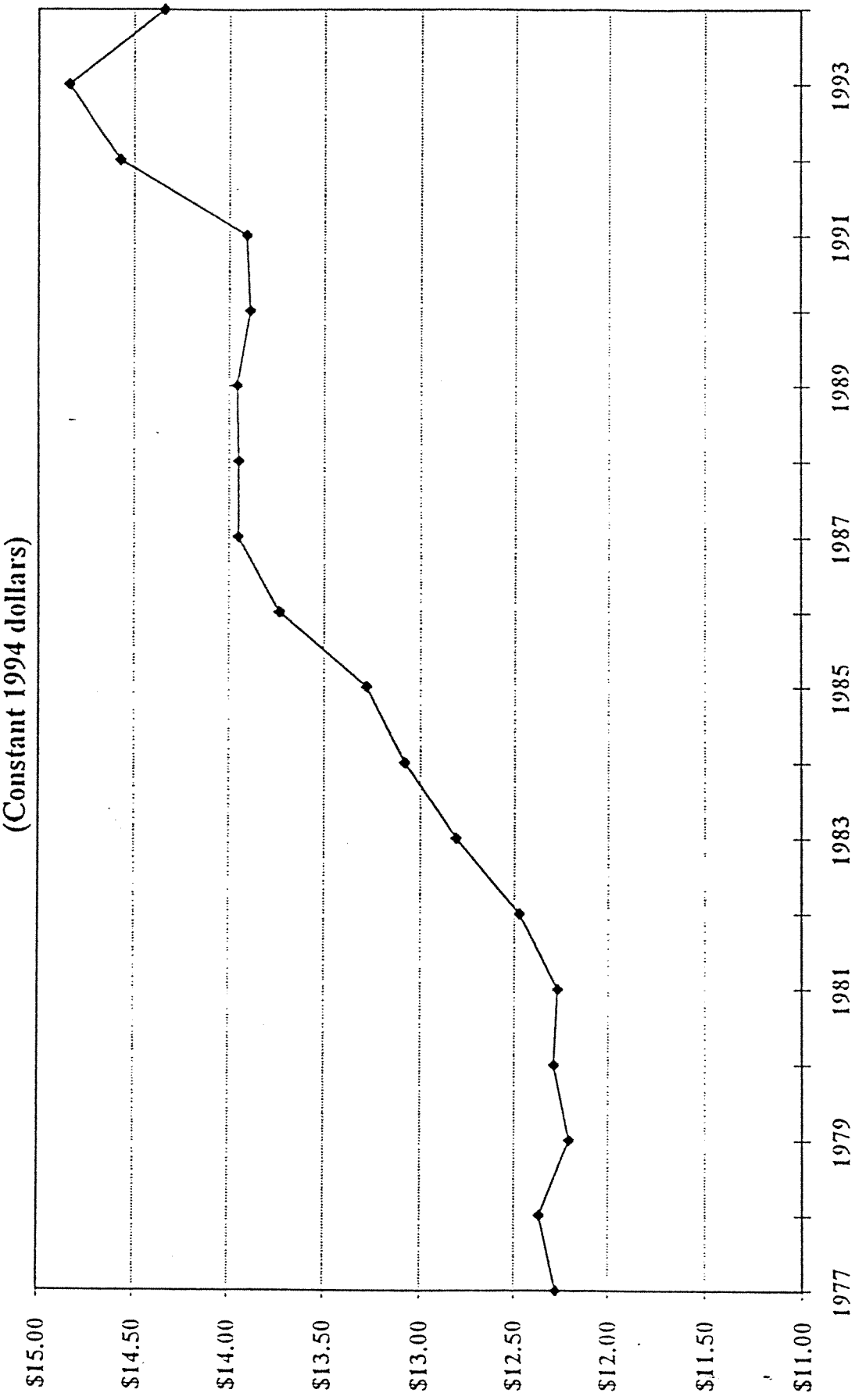
29. See, for example, "Summary of the UAW-Ford National Contract," Bureau of National Affairs, Inc. Daily Labor Reporter, Washington D.C., No. 184, September 24, 1993. The hourly wage for janitors was $17.85. Ford workers also earned a performance and Christmans bonus, usually between $2000 and $2,300.
30. Source: Semiconductor Industry Association, SIA Annual Databook: 1995.

Figure 3.8.3

Mean Hourly Earnings for Production Workers in Semiconductors, 1977-1994 (Constant 1994 dollars)

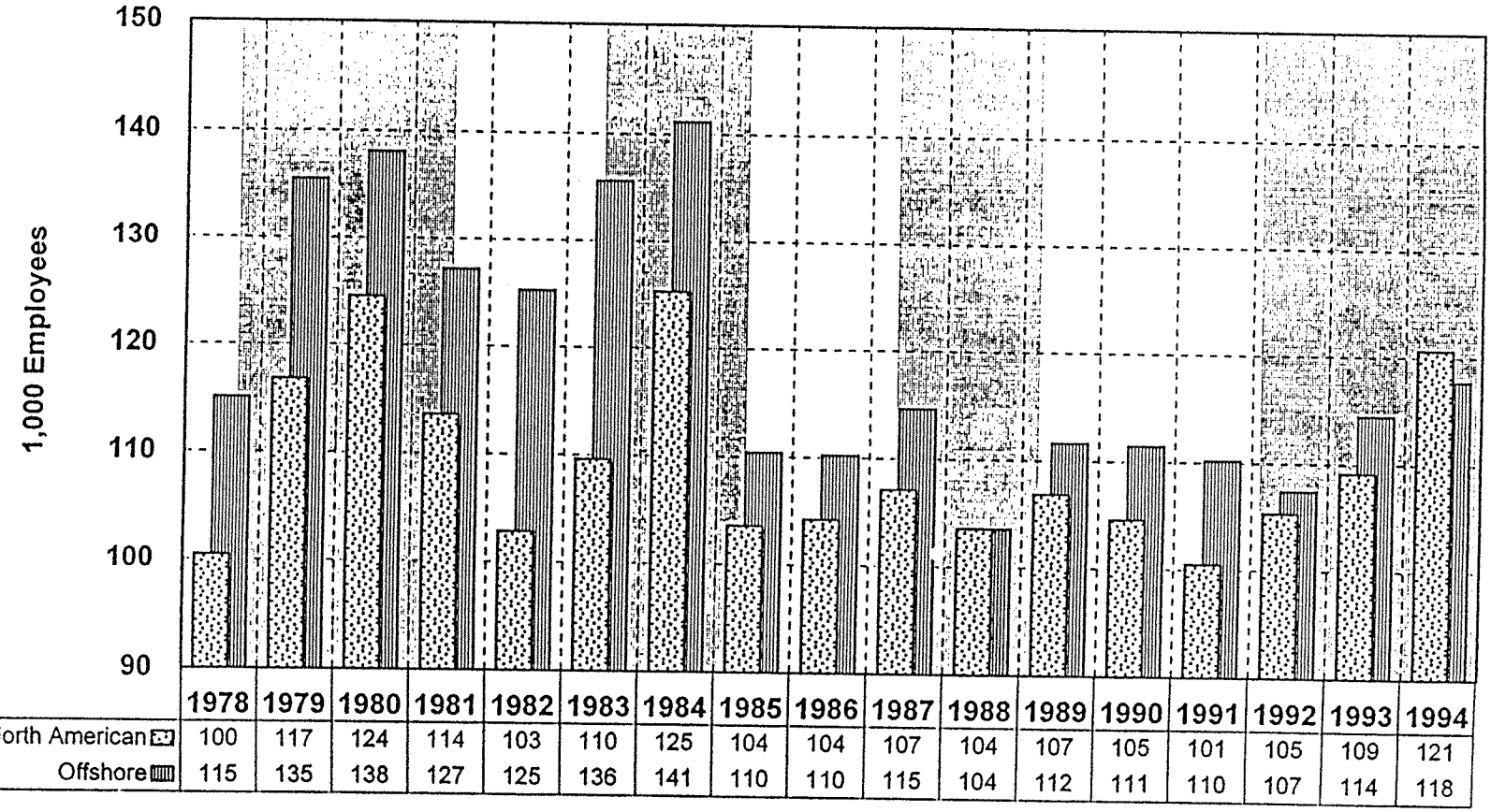


Source: Bureau of Labor Statistics

Figure 3.8.4
North American and Offshore Employment Levels

NORTH AMERICAN AND OFFSHORE EMPLOYMENT LEVELS

North American and offshore employment levels exhibit very similar cyclical patterns in response to market strength or weakness. There are no discernible differences between the responses of North American and offshore employment levels to periods of strong growth or weakness in the market.



	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994
North American	100	117	124	114	103	110	125	104	104	107	104	107	105	101	105	109	121
Offshore	115	135	138	127	125	136	141	110	110	115	104	112	111	110	107	114	118

SIA ANNUAL DATABOOK: 1995

4. Plans for the Continuing Survey
by Robert C. Leachman

Funded by the Alfred P. Sloan Foundation, the Competitive Semiconductor Manufacturing (CSM) program was initiated in 1991 as a multi-year research effort during which we planned to measure and analyze the performance of 25-30 wafer fabs. By the end of 1995, we had studied three fabs in a Pilot Phase and twenty eight fabs in the Main Phase. We are grateful for the cooperation we have received from the participants in measuring their manufacturing performance and documenting their practices, enabling us to identify key relationships between values of performance metrics and manufacturing practices as discussed in previous sections.

Our research funding from the Sloan Foundation will be exhausted before the end of 1996, and so a continuation of our competitive studies requires additional support and sponsorship. The Sloan Foundation has indicated to us that they will entertain a proposal requesting sponsorship of continued research concerning semiconductor manufacturing in two focus areas, with the understanding that we will seek full industry sponsorship for continued benchmarking studies. The focus areas we have selected include the following:

* Design and development for manufacturability, concerning the integration of product design, process development and transfer to mass production.

* Equipment efficiency improvement and factory automation, concerning techniques, practices and strategies to increase factory throughput.

Industry sponsorship of our competitive studies has already begun on a limited basis. We have received grants of $50,000 from Sematech and $25,000 each from the Electronics Industry Association of Japan (EIAJ) and the Semiconductor Industry Research Institute of Japan (SIRIJ). To continue the benchmarking studies, we will need additional sponsorship, which we intend to solicit during the remainder of 1996. Our goal is to obtain $200,000 per year in industry sponsorship of the competitive studies.

In connection with this transition to industry sponsorship, we need to solicit industry advice concerning future direction for the competitive studies. As we are able to secure increased industry funding, we plan to expand membership of our Industrial Advisory Board and to hold more frequent meetings of the Board.

The technical performance metrics we have developed (cycle time per wafer layer, line yield per 20 layers, defect densities, equipment throughputs, labor productivities, integrated yields and throughputs), while far from perfect, appear to be adequate to perform comparative analysis of the fabs in our survey. We have encountered a wide range of scores on every metric, spanning factors of 2, 4 or even 10. Thus the metrics are very effective at discriminating the participants. Almost all fabs we have visited use these same or similar metrics for internal performance evaluations, and thus the values of these metrics would seem to be of interest to them.

Our survey procedure to date has followed a basic cycle of receiving a completed Mail-Out Questionnaire from a participant, computing metric scores and trends, making a site visit by a team of 6-8 faculty and students to investigate underlying practices following a 2-day agenda sent to the participant, then documenting and discussing the findings of the visit, and ultimately comparing and writing up the findings as an interim report each time a group of 8-12 more visits have been completed. Before public release of the report, we give the participants two weeks to read a

draft and comment.

As our survey has become mature, we have asked past participants fill out the Mail-Out Questionnaire about once every two years so that we may update their metric scores. We do not plan to re-visit them unless there has been a substantial and inexplicable change in scores, indicating a significant change has been made in practices. In the long run, if the number of participants becomes large, we may consider being selective about making site visits to new participants, visiting only those with unusual scores or those who feel they have some unique practices to share with us.

Like our participants, we must strive for continuous improvement in the execution of our survey processes. Comments and suggestions from industry and academia are always welcome.

Appendix A. CSM Main Phase Staff and Industrial Advisory Board

The Competitive Semiconductor Manufacturing (CSM) Program is a multi-year, interdisciplinary research program jointly undertaken by the Haas School of Business, the College of Engineering and the Berkeley Roundtable on the International Economy of the University of California at Berkeley. The Program has an Advisory Board including executives from many leading semiconductor manufacturers from around the world and is funded by the Alfred P. Sloan Foundation of New York.

The CSM program includes a Main Phase survey (the results of which are described in this report) as well as several Focus Studies on technical and managerial topics worthy of deeper investigation. Listed below are the members of the Industrial Advisory Board, and the faculty, graduate student and professional staff working on the Main Phase survey of the first sixteen participants.

Main Phase Research Staff

David A. Hodges, Dean, College of Engineering, and Project Co-Director.

Robert C. Leachman, Professor of Industrial Engineering and Operations Research, Project Co-Director and Team Leader for all site visits.

Vinay S. Sohoni, Adjunct Professor of Industrial Engineering and Operations Research, on teams for 10 site visits.

Katalin Voros, Manager of the U.C. Berkeley Microfabrication Laboratory, on teams for 10 site visits.

David Mowery, Associate Professor of Business Administration, on teams for 5 site visits.

Rajan Srikanth, Assistant Professor of Business Administration, on teams for 10 site visits.

C. Neil Berglund, Professor of Electrical Engineering at the Oregon Graduate Institute, on teams for 7 site visits.

Clair Brown, Professor of Economics, on teams for 4 site visits.

Chien Hwa Wang, Post-doctoral scholar in Industrial Engineering and Operations Research, on teams for 4 site visits.

Costas Spanos, Professor of Electrical Engineering and Faculty Director of the U.C. Berkeley Microfabrication Laboratory, on teams for 3 site visits.

J. George Shanthikumar, Professor of Business Administration, on teams for 3 site visits.

David Bowen, Lecturer in Industrial Engineering and Operations Research, on 3 site visit

teams.

Michael Borrus, Co-Director, Berkeley Roundtable on the International Economy, on teams for 2 site visits.

Stefan Reichelstein, Professor of Business Administration, on teams for 2 site visits.

Lawrence Rowe, Professor of Computer Science, on teams for 2 site visits.

C. Roger Glassey, Professor of Industrial Engineering and Operations Research, on teams for 2 site visits.

John Fowler, Asst. Professor of Industrial Engineering at Arizona State University, on one site visit team.

Michael Reich, Professor of Economics, on one site visit team.

Susan Billat, President, Benchmarking Strategies, Inc., on one site visit team.

Sean Cunningham, graduate student in Industrial Engineering and Operations Research, on teams for 19 site visits.

Robert Benson, graduate student in Industrial Engineering and Operations Research, on teams for 17 site visits.

Melissa M. Appleyard, graduate student in Economics, on teams for 10 site visits.

Baruch Saeed, graduate student in Industrial Engineering and Operations Research, on teams for 8 site visits.

Eric Thacker, graduate student in Business Administration, on teams for 8 site visits.

Nile Hatch, graduate student in Agricultural and Resource Economics, on teams for 7 site visits.

Thomas Sloan, graduate student in Business Administration, on teams for 6 site visits.

Amy Shuen, graduate student in Business Administration, on teams for 6 site visits.

Jumbi Edulbehram, graduate student in City and Regional Planning, on teams for 6 site visits.

George McMurray, graduate student in Industrial Engineering and Operations Research, on teams for 5 site visits.

Maureen Lojo, graduate student in Business Administration (MIT), on teams for 5 site visits.

Linda Sattler, graduate student in Industrial Engineering and Operations Research, on teams for 5 site visits.

Veronica Wu, graduate student in Industrial Engineering and Operations Research, on teams for 4 site visits.

Vincent Valvano, graduate student in Economics, on teams for 3 site visits.

Jackson Nickerson, graduate student in Business Administration, on teams for 3 site visits.

Paolo Palezzato, graduate student in Industrial Engineering and Operations Research, on teams for 3 site visits.

Ting-yun Liu, graduate student in Industrial Engineering and Operations Research, on teams for 2 site visits.

Jeenyoung Kang, graduate student in Industrial Engineering and Operations Research, on teams for 2 site visits.

Tali Carmon, graduate student in Industrial Engineering and Operations Research, on teams for 2 site visits.

Dan Rascher, graduate student in Economics, on one site visit team.

Adeel Najmi, graduate student in Industrial Engineering and Operations Research, on one site visit team.

Janet Berkovitz, graduate student in Business Administration, on one site visit team.

Ken Bowers, project Administrative Assistant.

Celeste Newbrough, Publications Coordination

Eric Rutledge, U. C. Berkeley Tokyo Office, Japanese interpretor and coordinator for site visits in Japan.

Selma Monsky, U. C. Berkeley Survey Research Center, layout of Mail-Out Questionnaire

Hirotsugu Matoba, Visiting Scholar from Sharp Corporation, translation of Mail-Out Questionnaire into Japanese.

Kumiko Tabata, translation of business cards into Japanese.

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